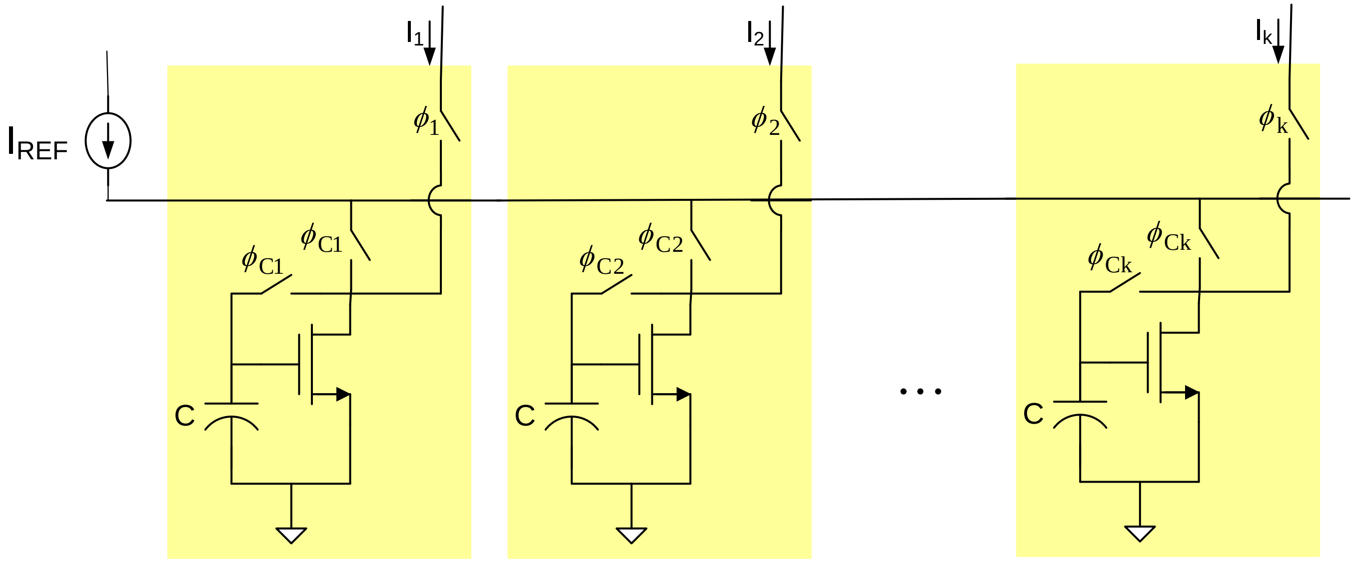
EE 505

Lecture 18

Architectural Performance Comparisons

ADC Design

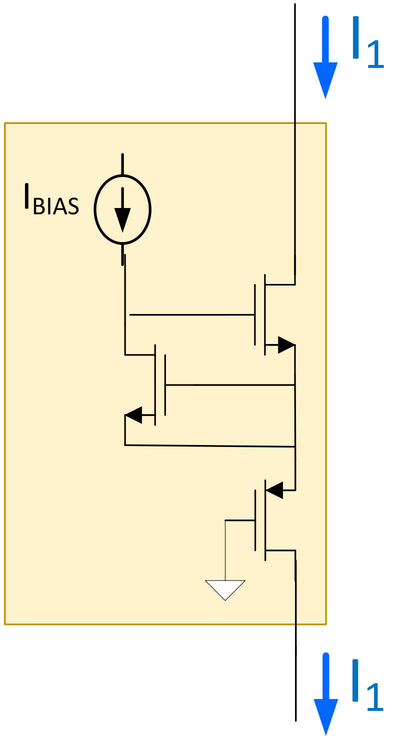
Dynamic Current Source Matching



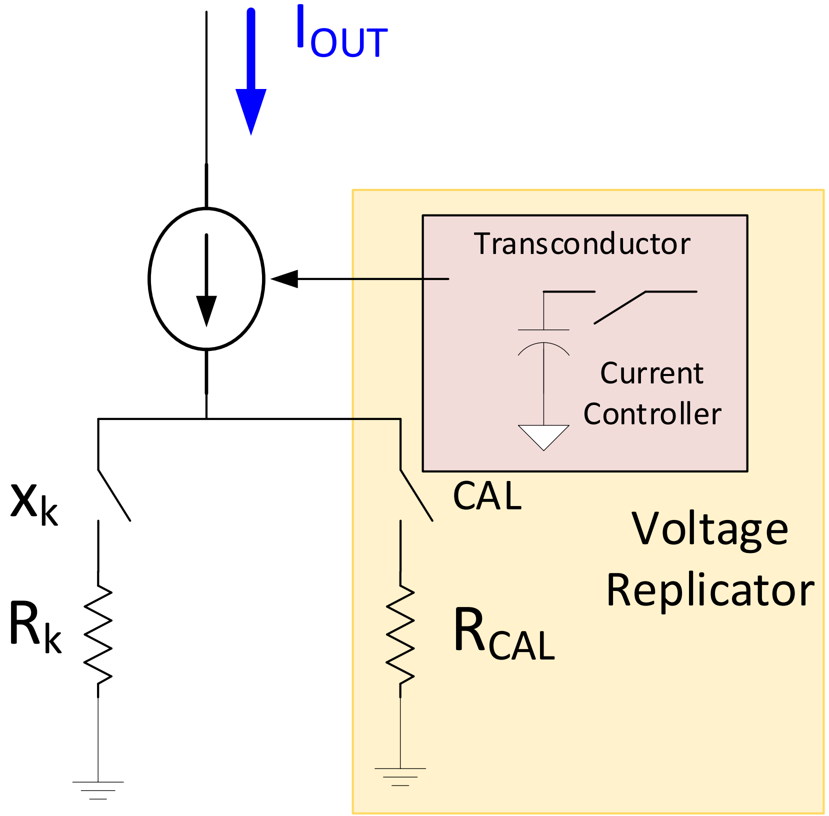
- Correct charge is stored on C to make all currents equal to I_{REF}
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on C
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer or binary coded)
- Still use steering rather than switching in DAC

Often termed "Current Copier" or "Current Replication" circuit

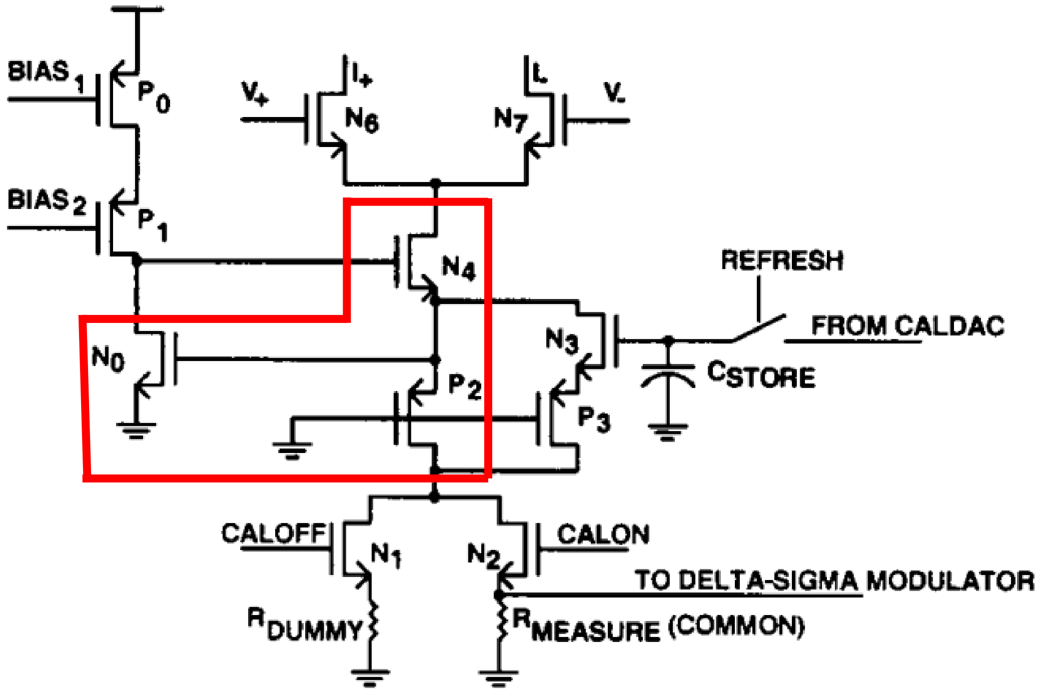
Floating Current Source



Floating Current Copier



Another Dynamic Current Source Matching Structure



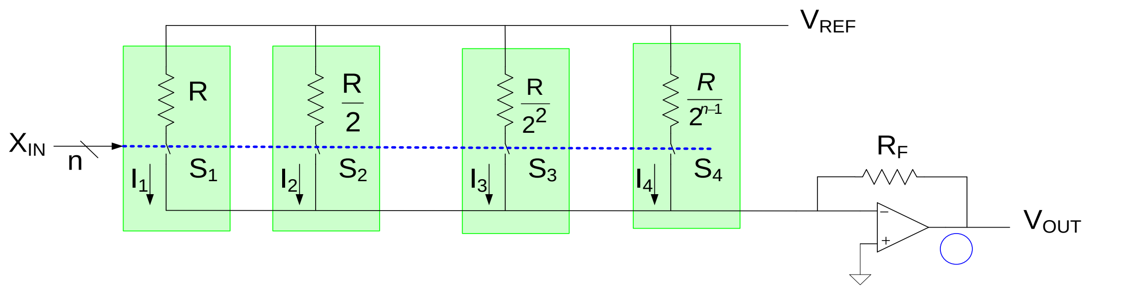
Floating Current Source

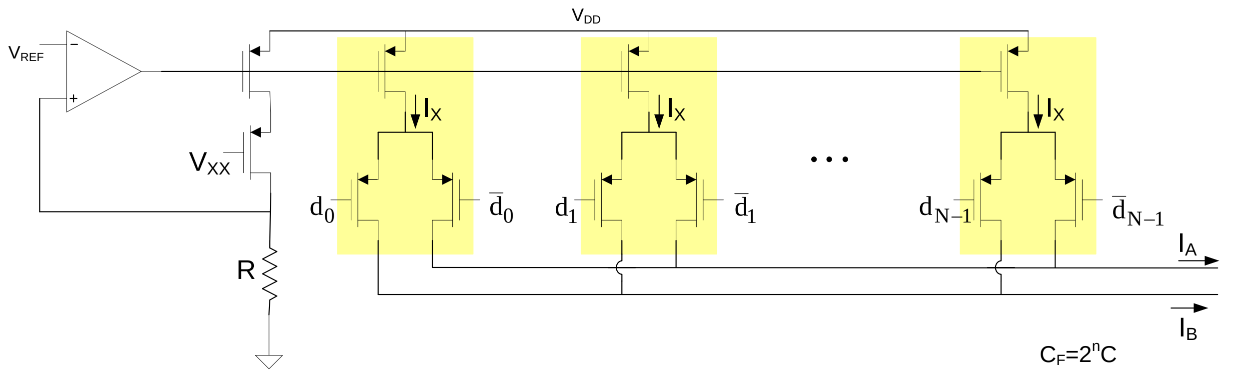
Voltage Copier

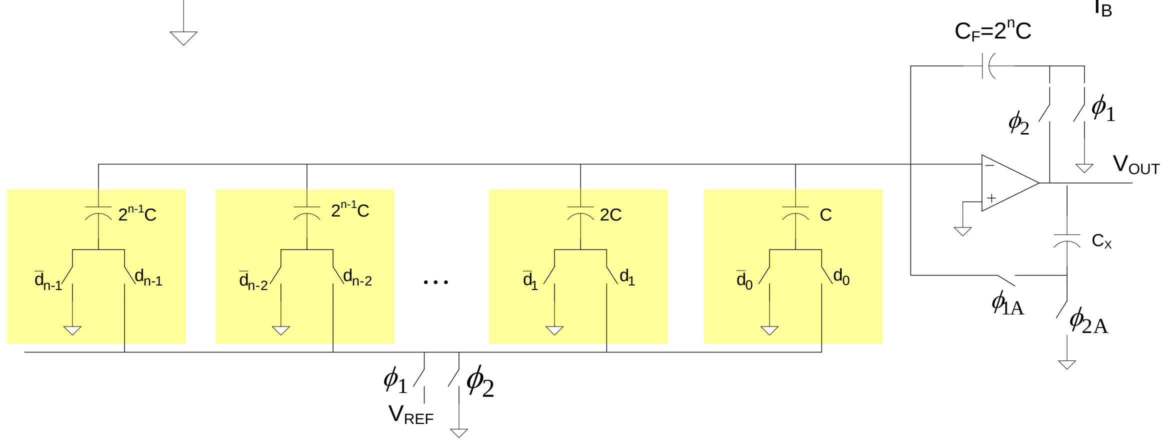
Eliminates need to remove current source from circuit during cal

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?



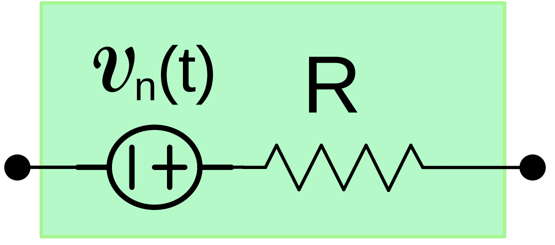




Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in resistors:



Noise spectral density of $v_n(t)$ at all frequencies $S = 4kTR$

This is white noise !

k: Boltzmann's Constant
T: Temperature in Kelvin

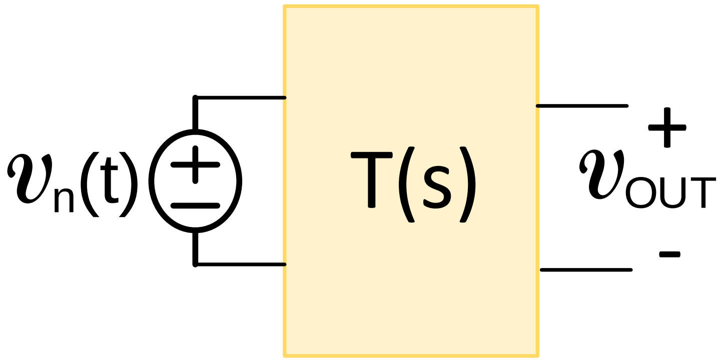
$k=1.38064852 \times 10^{-23}\ m^2\ kg\ s^{-2}\ K^{-1}$

At 300K, $kT=4.14 \times 10^{-21}$

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in linear circuits:

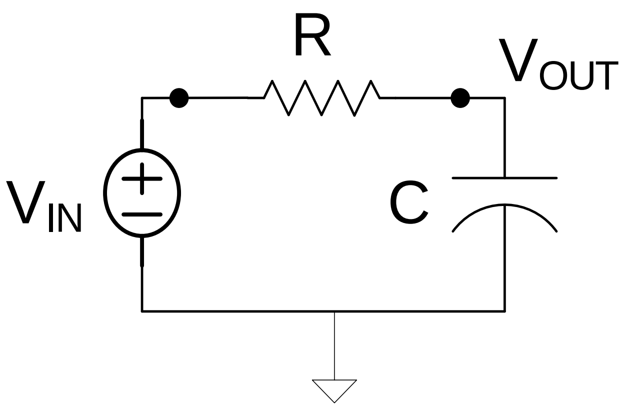


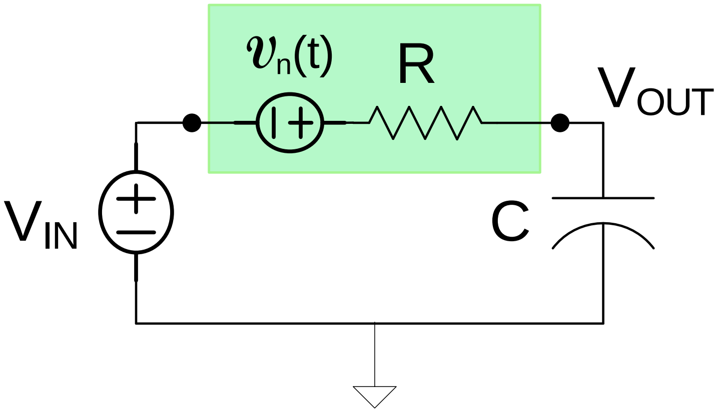
Due to any noise voltage source:

$$S_{V_{OUT}} = S_{V_n} \left| T(j\omega) \right|^2$$

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \sqrt{\int_{f=0}^{\infty} S_{V_n} \left| T(j\omega) \right|^2 df}$$

Example: First-Order RC Network





$$T(s) = \frac{1}{1+RCs}$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\, df}$$

Useful Trig Identity:

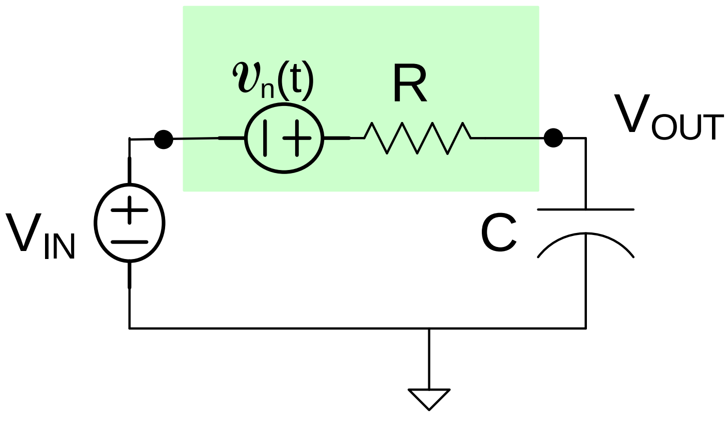
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, \mathrm{df}} = \sqrt{\int_{f=0}^{\infty} \frac{4\mathrm{kTR}}{1+\omega^2 \mathrm{R}^2 \mathrm{C}^2} \mathrm{df}} = \sqrt{\frac{4\mathrm{kT}}{\mathrm{RC}^2} \int_{f=0}^{\infty} \frac{1}{\left(\frac{1}{\mathrm{RC}}\right)^2 + \omega^2} \mathrm{df}}$$

$$\int_{x=0}^{\infty} \frac{1}{a^2 + x^2} dx = \frac{\pi}{2a}$$

If $\omega = 2\pi \mathbf{f}$ this can be rewritten as

$$\int_{f=0}^{\infty} \frac{1}{b^2 + \omega^2} df = \frac{1}{4b}$$

Example: First-Order RC Network

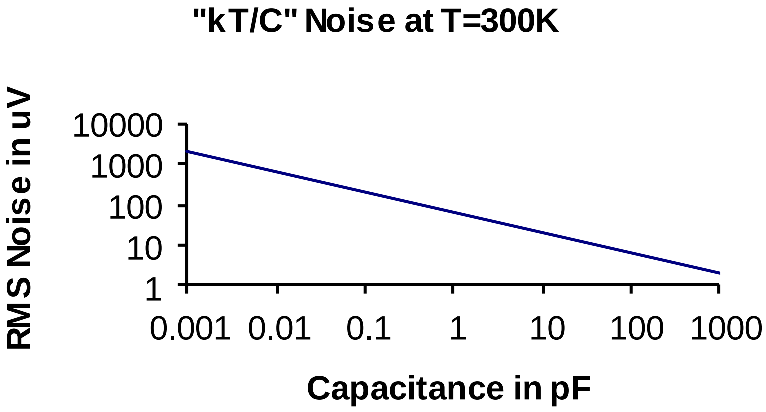


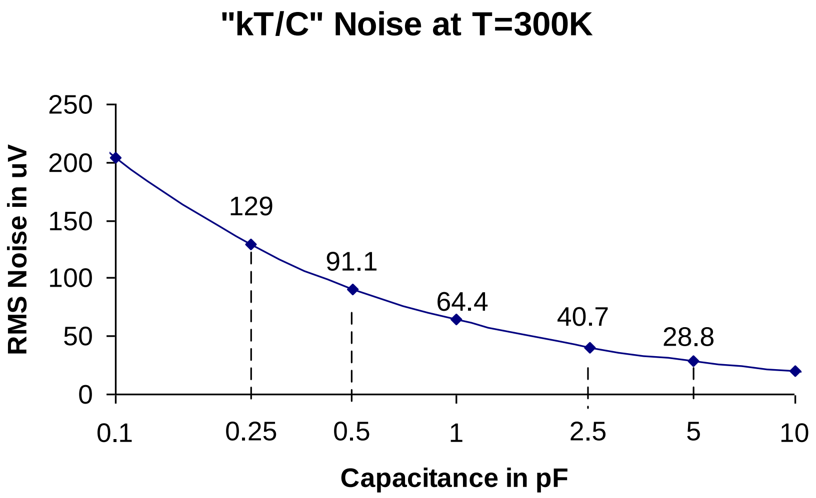
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2 R^2 C^2}\, df}$$

From a standard change of variable with a trig identity, it follows that

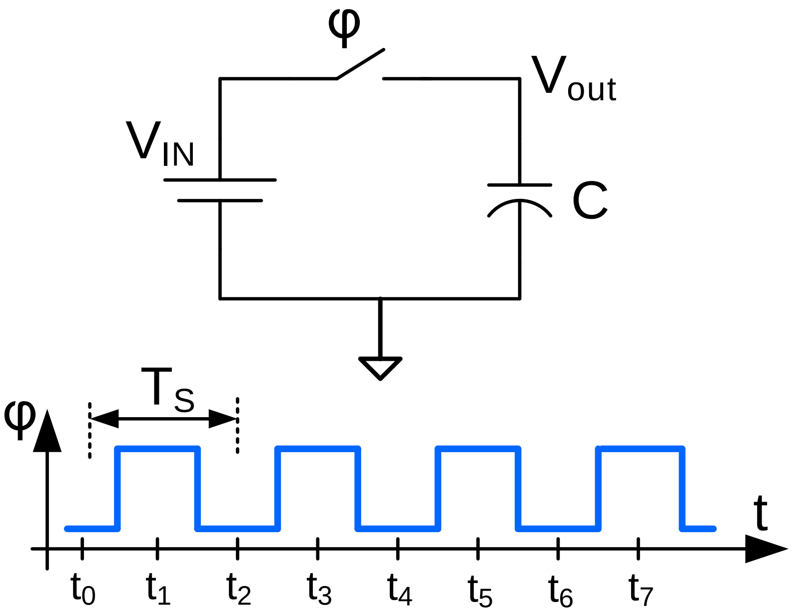
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$

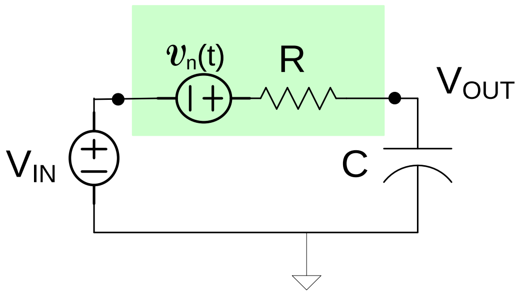
- The continuous-time noise voltage has an RMS value that is independent of R
- Noise contributed by the resistor is dependent only upon the capacitor value C
- This is often referred to at kT/C noise and it can be decreased at a given T only by increasing C


"kT/C" Noise at T=300K
RMS Noise in uV
10000
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Capacitance in pF

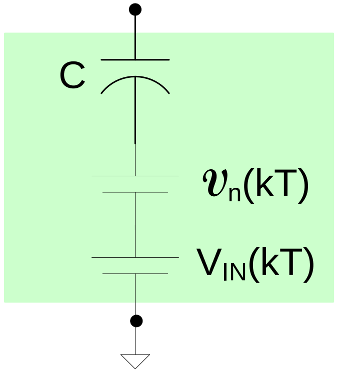

"kT/C" Noise at T=300K
RMS Noise in uV
250
200
150
100
50
0
129
91.1
64.4
40.7
28.8
0.1
0.25
0.5
1
2.5
5
10
Capacitance in pF

Example: Switched Capacitor Sampler



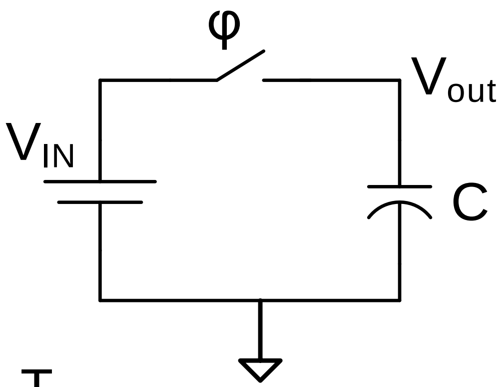


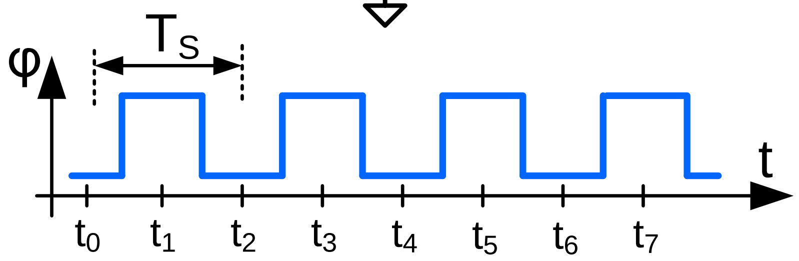
Track mode

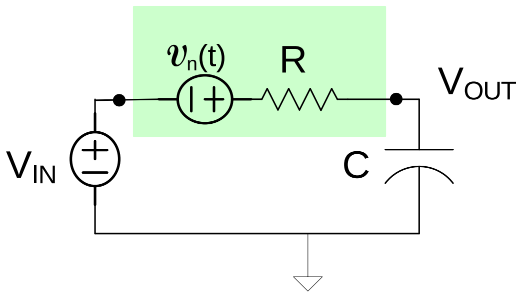


Hold mode

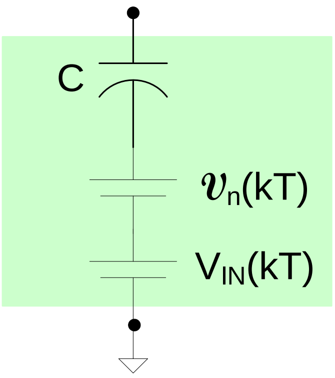
Example: Switched Capacitor Sampler







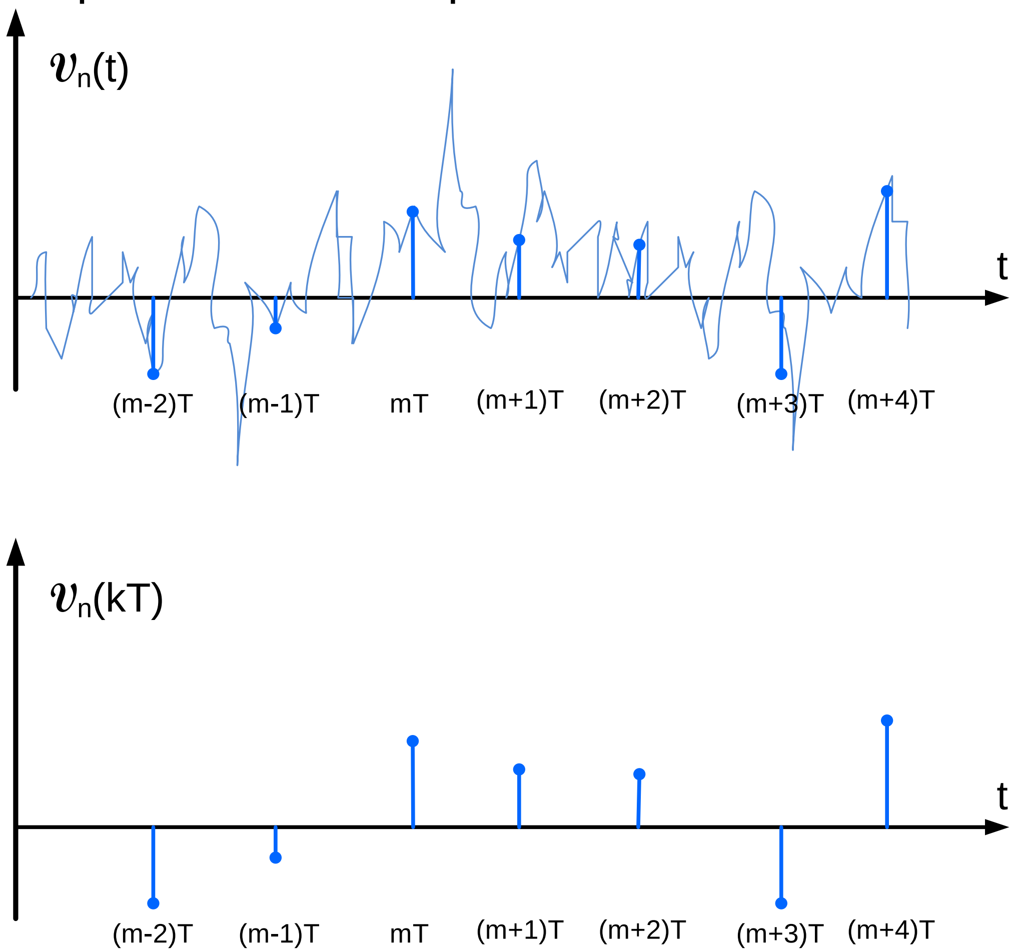
Track mode



Hold mode

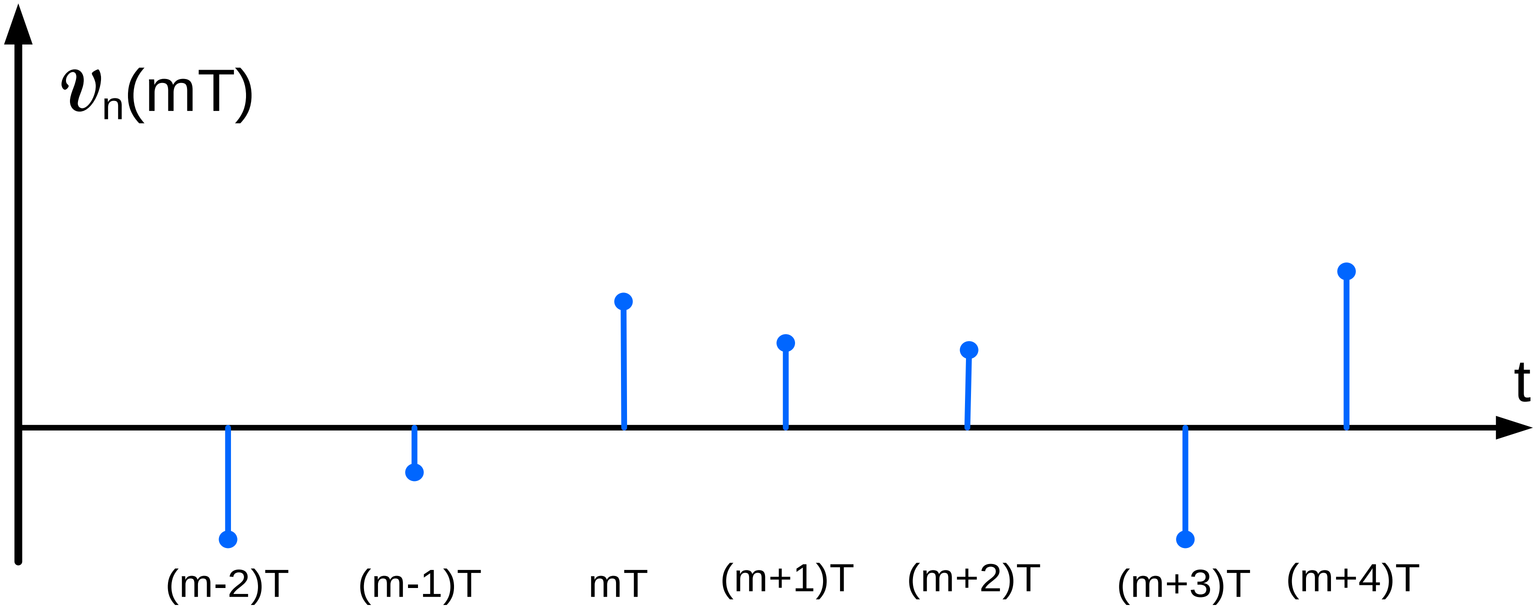
Example: Switched Capacitor Sampler

T is the period of the sampler



$v_n(mT)$ is a discrete-time sequence obtained by sampling continuous-time noise waveform

Characterization of a noise sequence

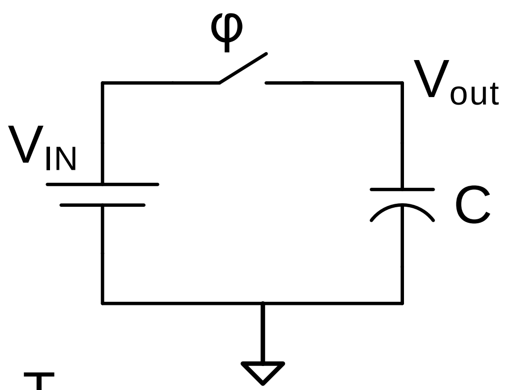


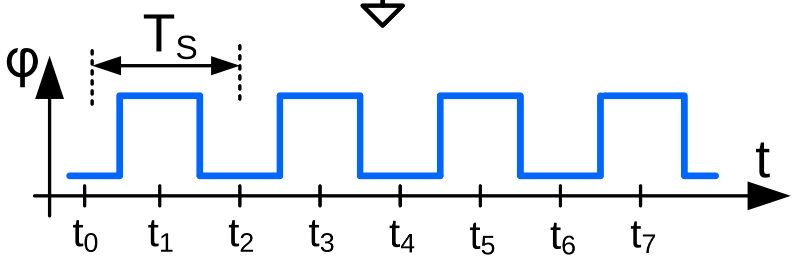
$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right) \underset{N\ large}{\simeq} \sqrt{\frac{1}{N}\sum_{m=1}^{N} v^2(mT)}$$

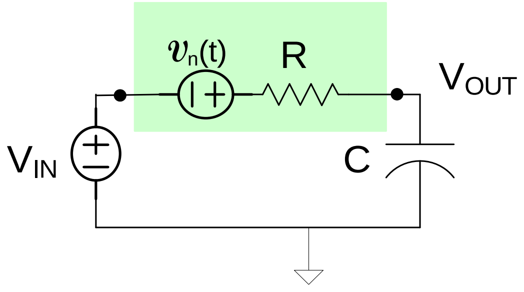
Theorem If $\mathcal{V}(t)$ is a continuous-time zero-mean noise source and $<\mathcal{V}(kT)>$ is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as $\mathcal{V}_{RMS} = \hat{\mathcal{V}}_{RMS}$

Theorem If $\mathcal{V}(t)$ is a continuous-time zero-mean noise signal and $<\mathcal{V}(kT)>$ is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the standard deviation of the random variable $\mathcal{V}(kT)$, denoted as $\sigma_{\hat{V}}$ satisfies the expression $\sigma_{\hat{V}} = \mathcal{V}_{RMS} = \hat{\mathcal{V}}_{RMS}$

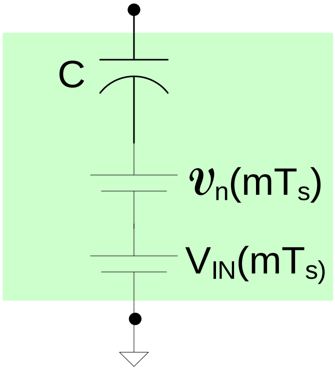
Example: Switched Capacitor Sampler







Track mode



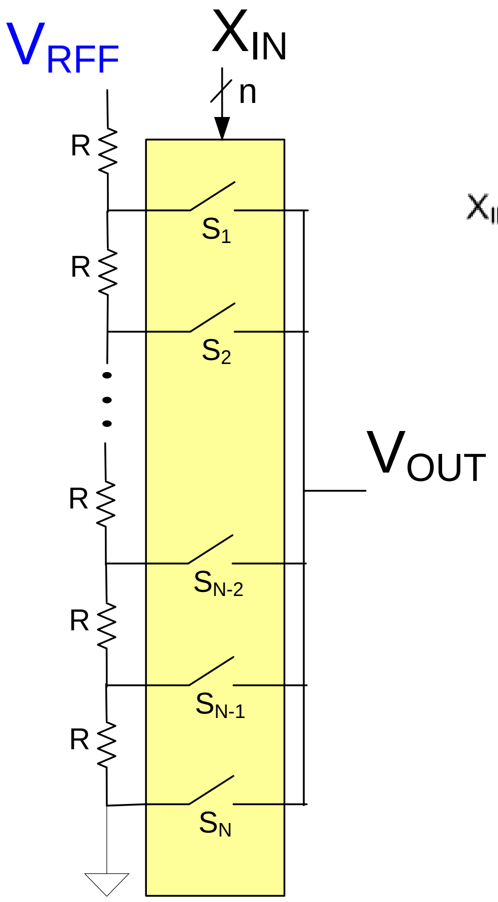
Hold mode

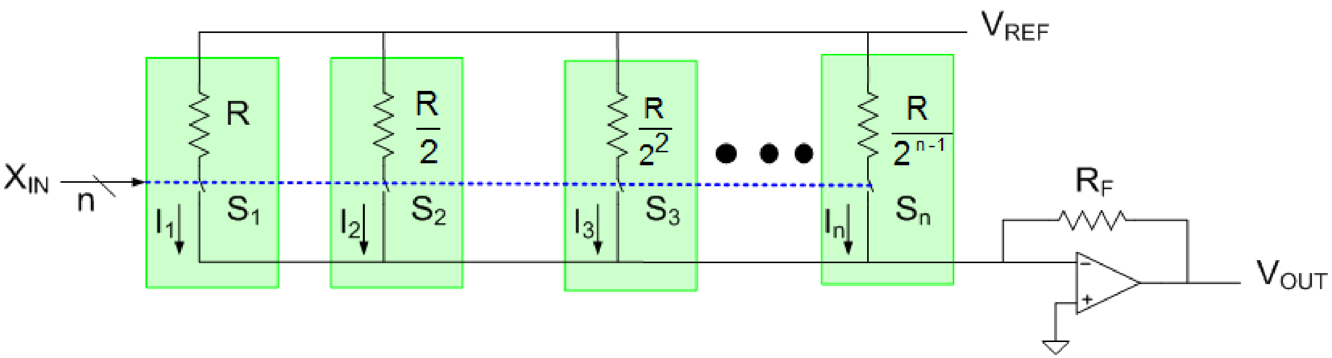
$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

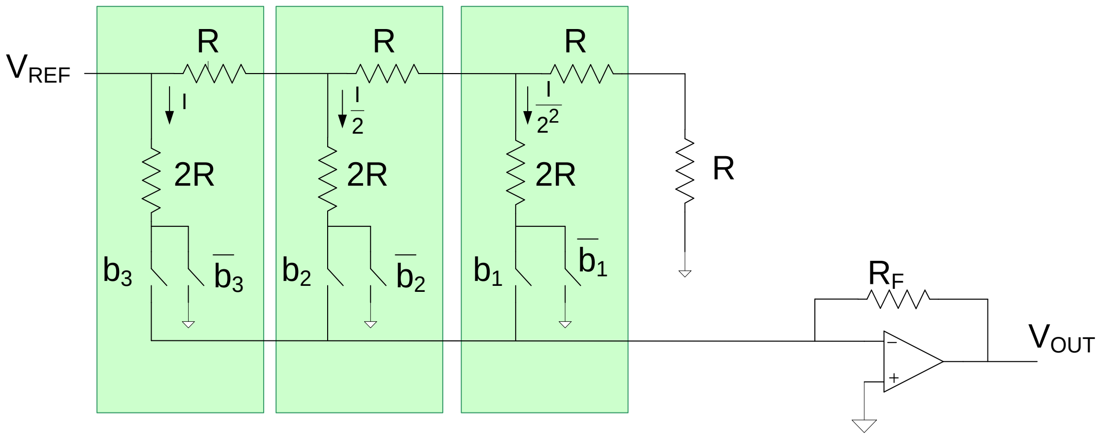
k: Boltzmann's constant
T: temperature in Kelvin

Architectural Performance Characterizations

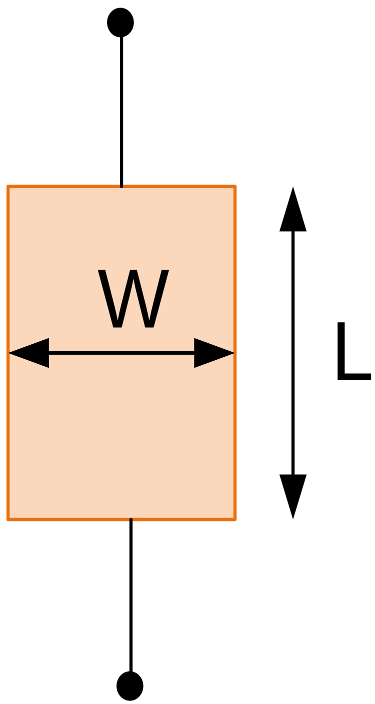
For the same total resistor area and the same resolution, how do these structures compare from a statistical characterization viewpoint?







Relative Statistical Characterization of R-based DACs



$$A = WL$$

$$\sigma_{\frac{R}{R_N}} = \frac{A_{\rho R}}{\sqrt{A}}$$

Relative Statistical Characterization of R-based DACs

For the same total area and the same resolution, how do these structures compare from a statistical characterization viewpoint?

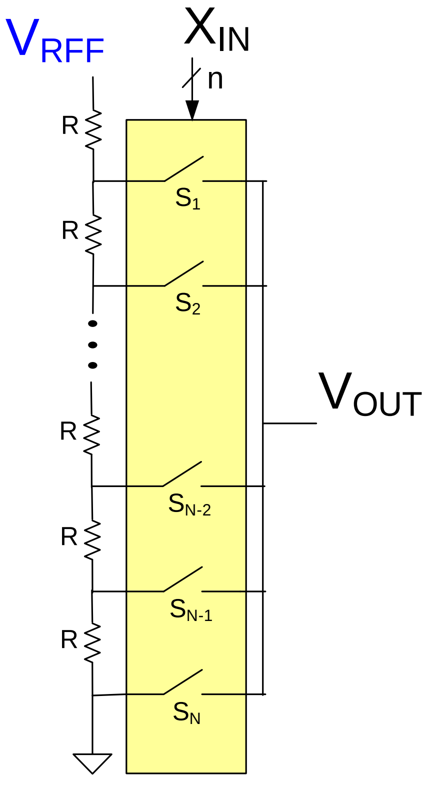
Simulation environment:

Resolution = 10
$A_{\rho R}$ = 0.02μm
Rnom = 1000
Area Unit Resistor = 2μm^2
Resistor Sigma= 14.1421
INLtarget = 0.5000 LSB

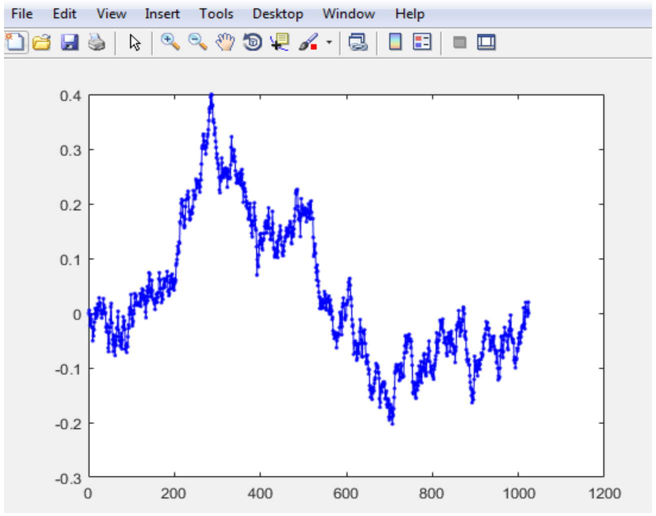
Yield: Must meet INL target

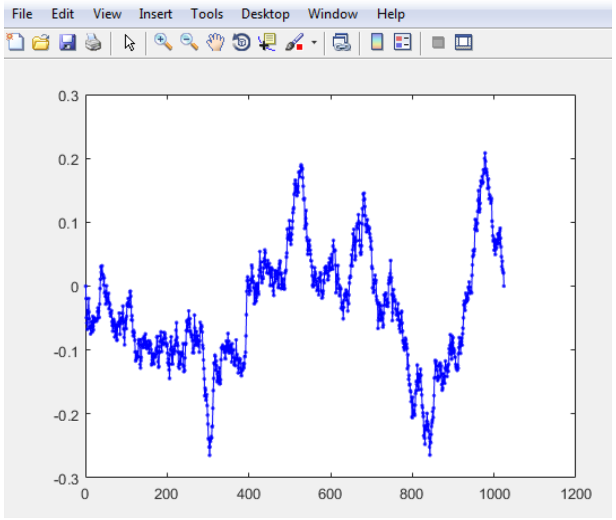
Relative Statistical Characterization of R-based DACs

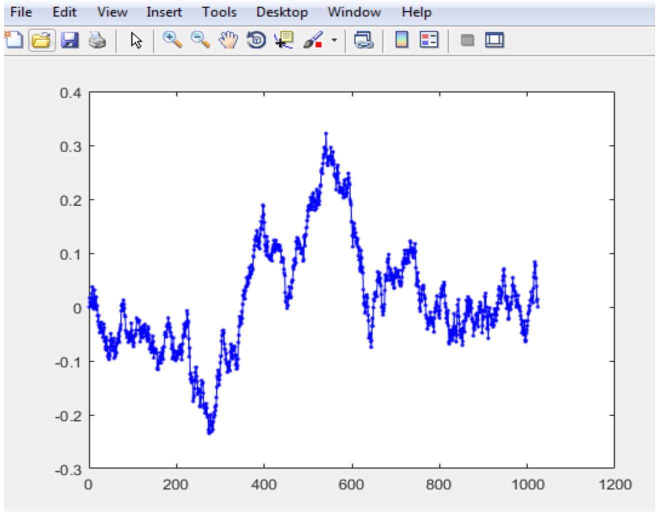
INL_k for four random implementations

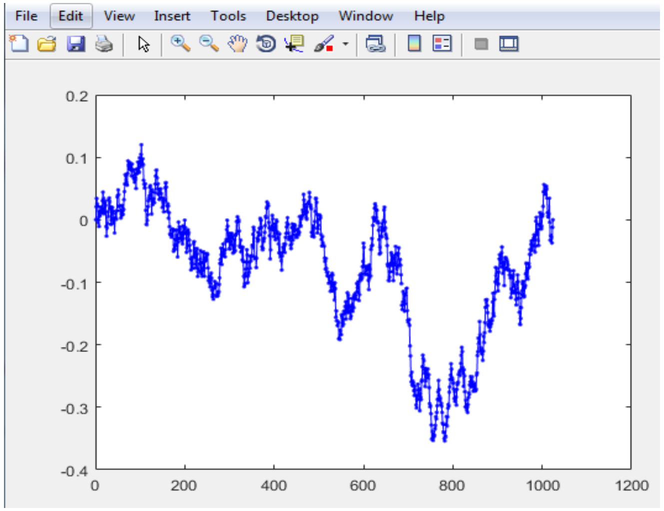


String DAC



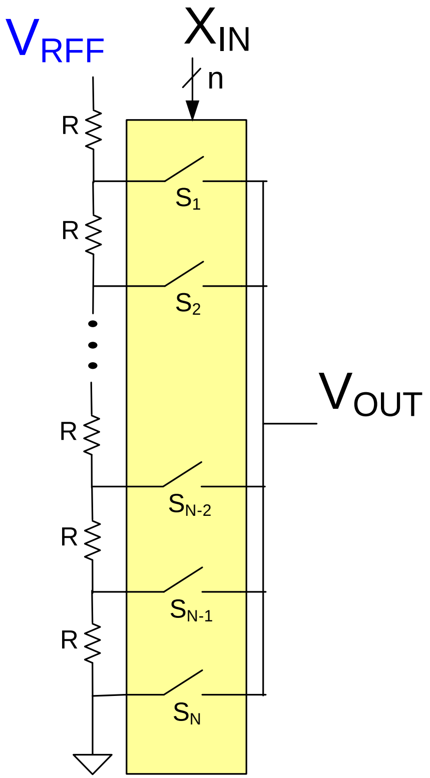




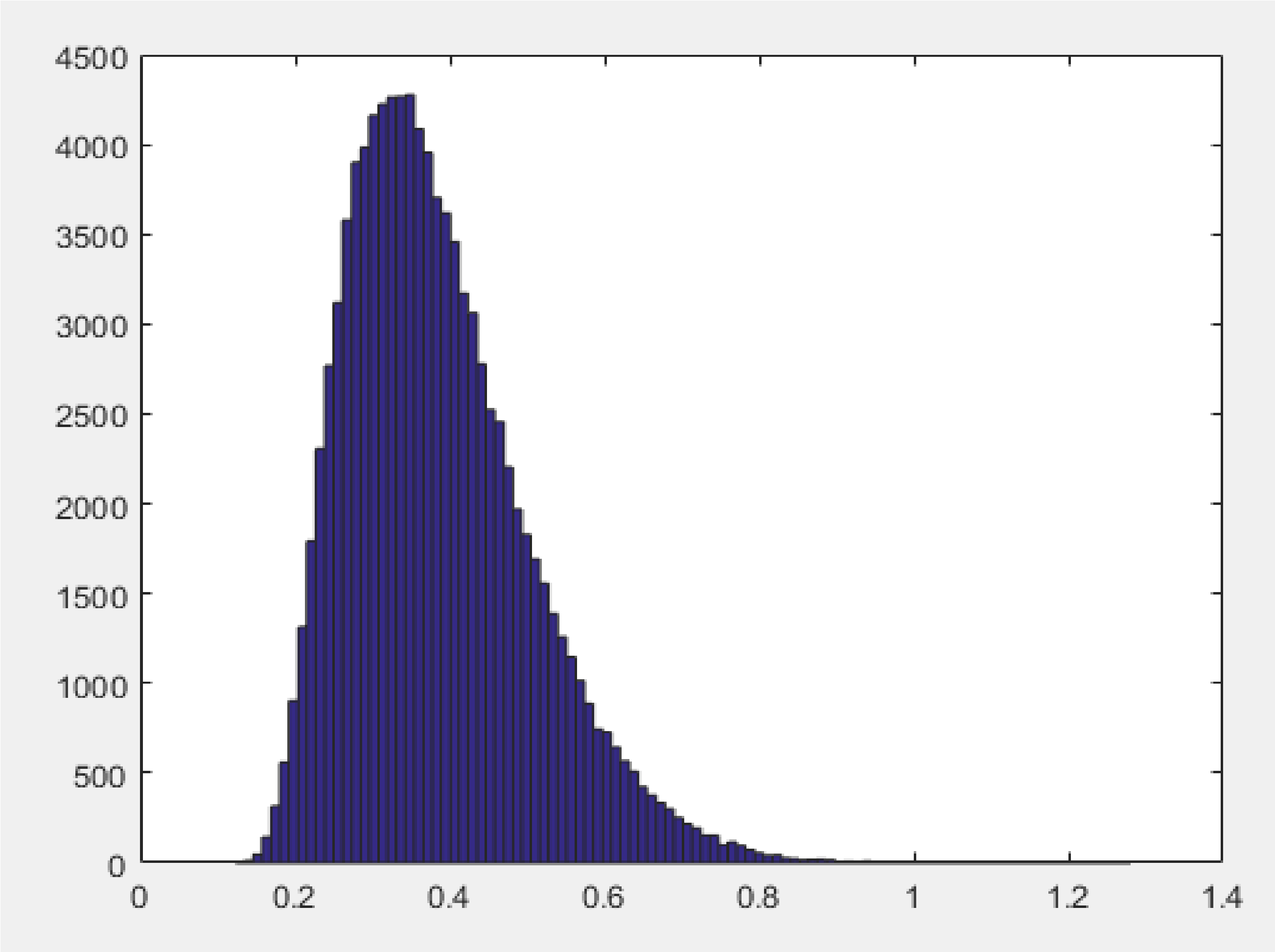


Relative Statistical Characterization of R-based DACs

INL histogram for 100,000 random implementations

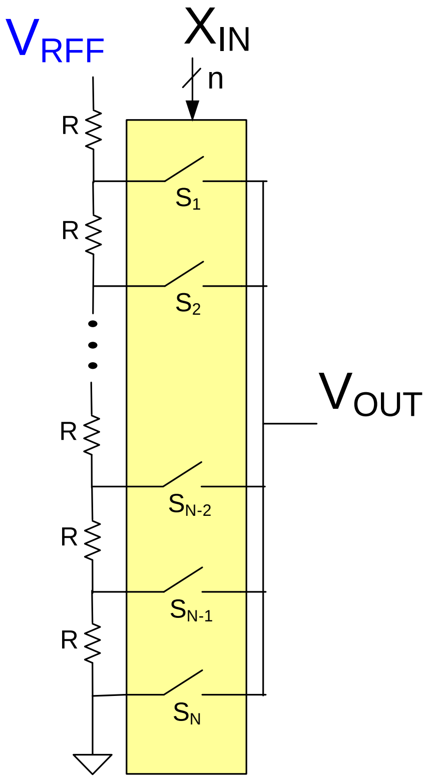


String DAC

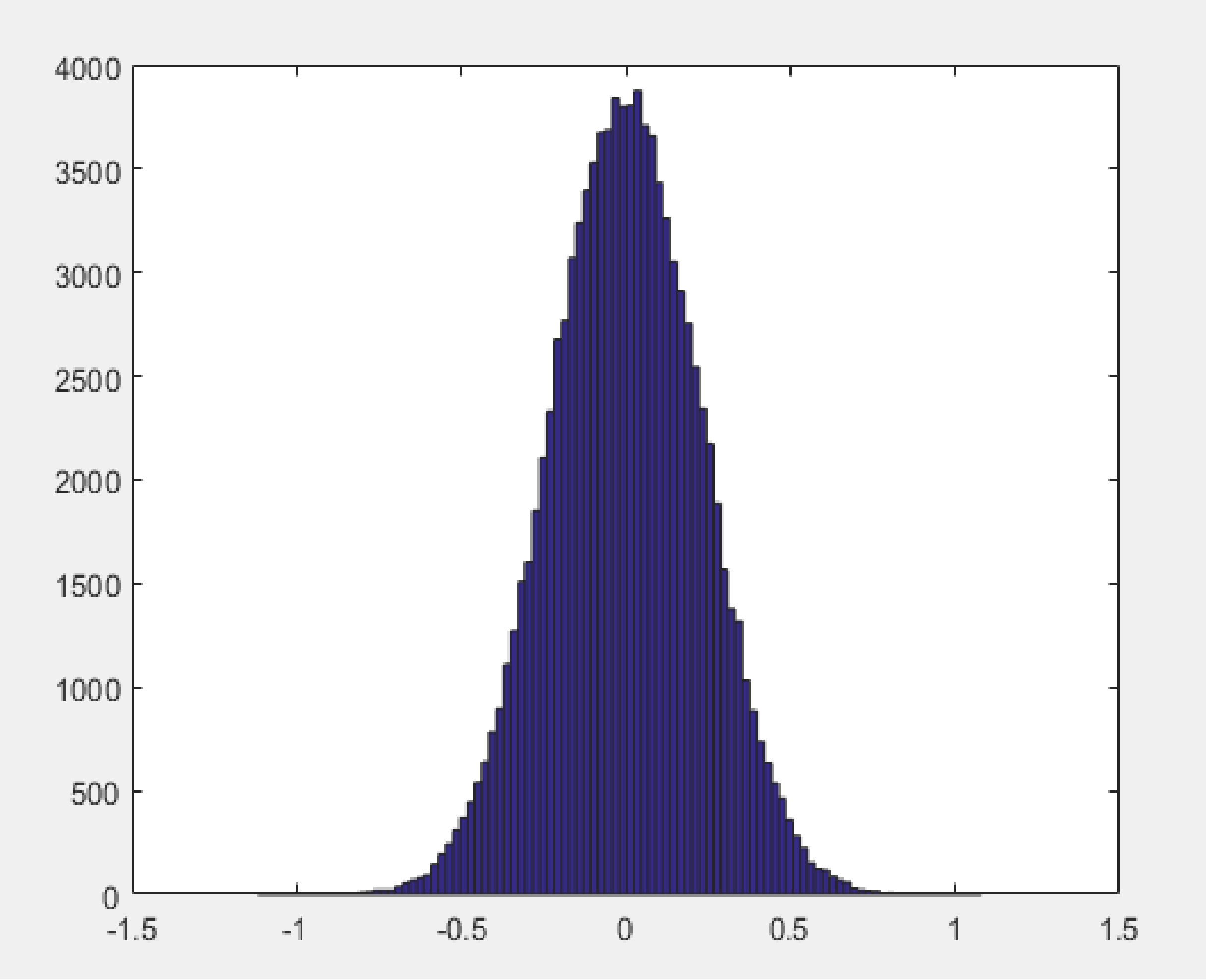


Relative Statistical Characterization of R-based DACs

INL_{kMAX} histogram for 100,000 random implementations

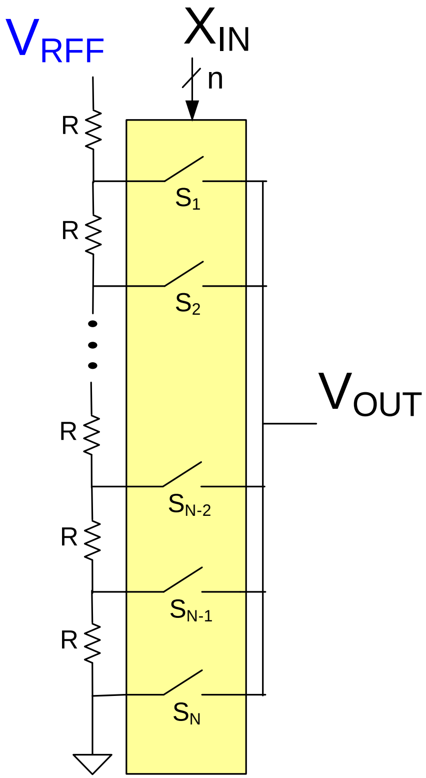


String DAC

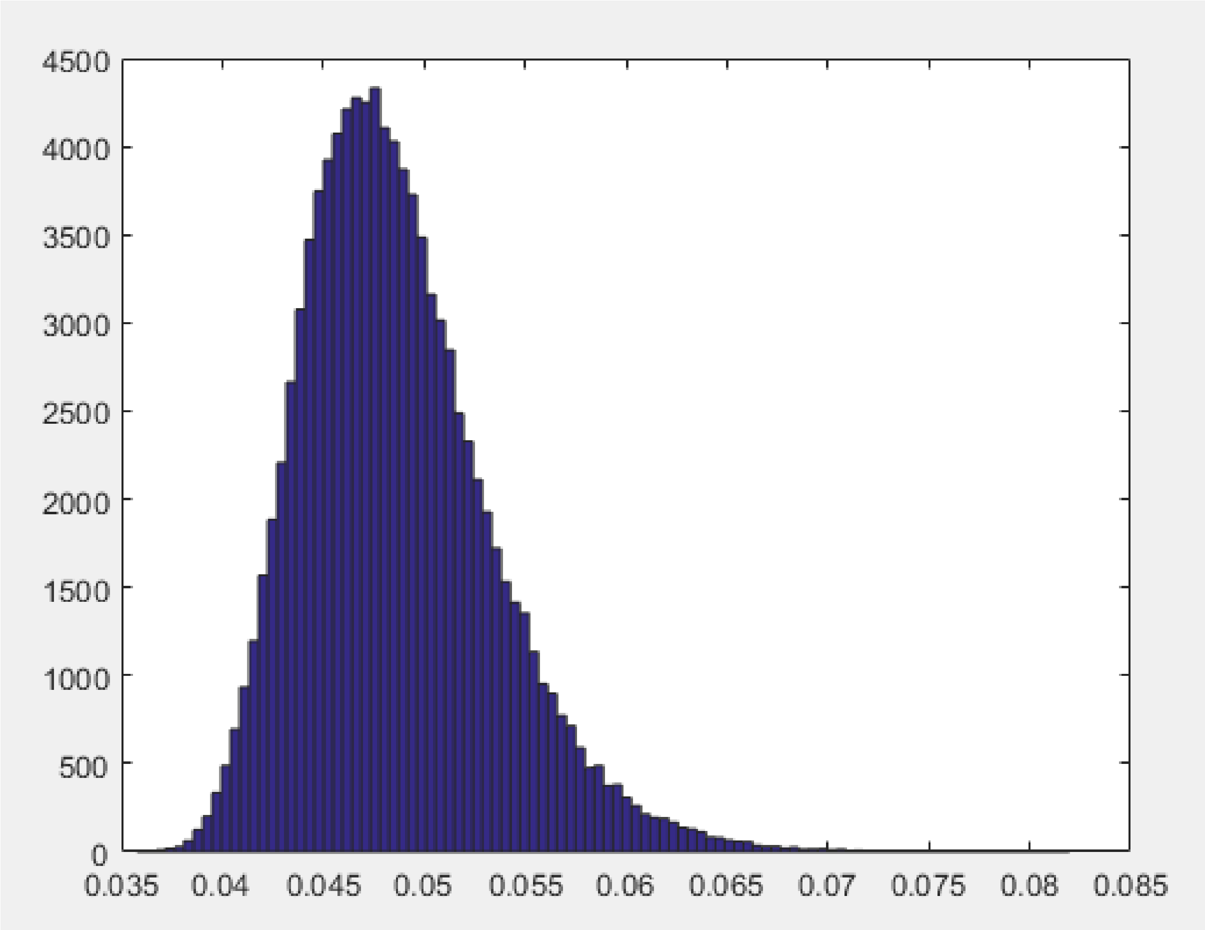


Relative Statistical Characterization of R-based DACs

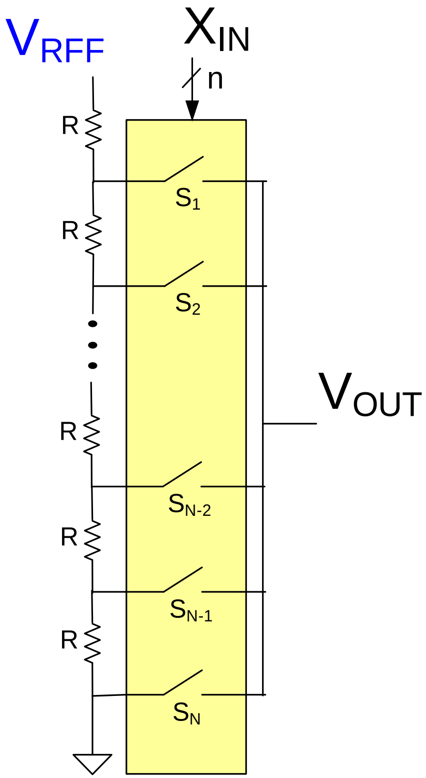
DNL histogram for 100,000 random implementations



String DAC



Relative Statistical Characterization of R-based DACs



String DAC

Summary

Resolution = 10

$A_{\rho R}$ = 0.02μm

R_{nom} = 1000

Area Unit Resistor = 2μm^2

Resistor Sigma= 14.1421

INL_{mean} = 0.385 LSB

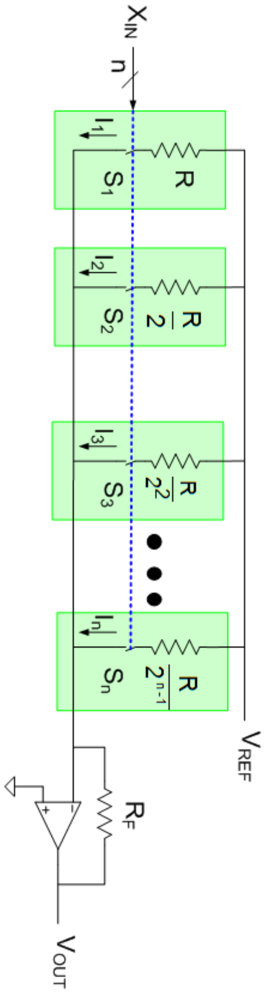
INL_{sigma} = 0.118 LSB

DNL_{mean} = 0.049 LSB

DNL_{sigma} = 0.0047 LSB

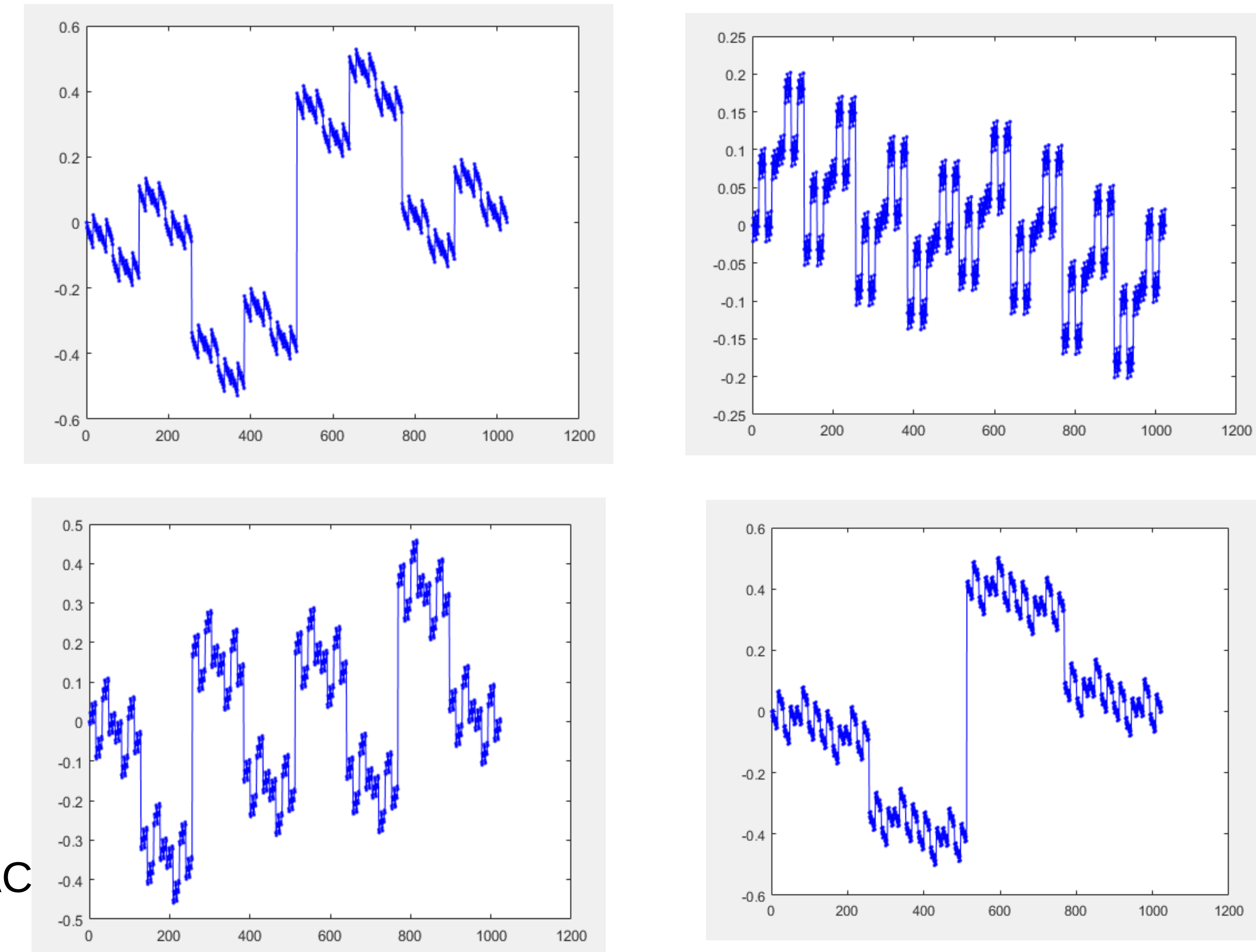
Yield (%) = 84.0

Relative Statistical Characterization of R-based DACs



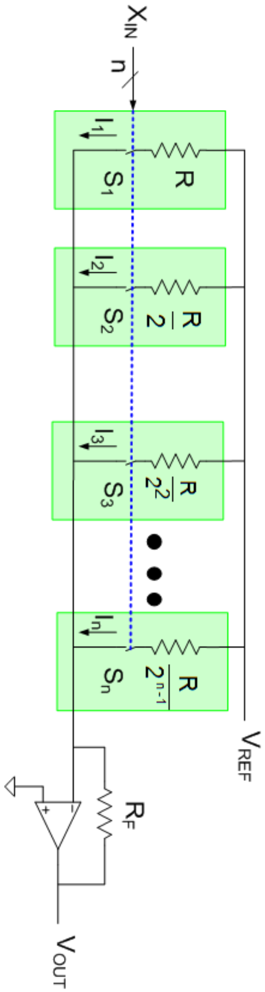
Binary Weighted DAC

INL_k for four random implementations

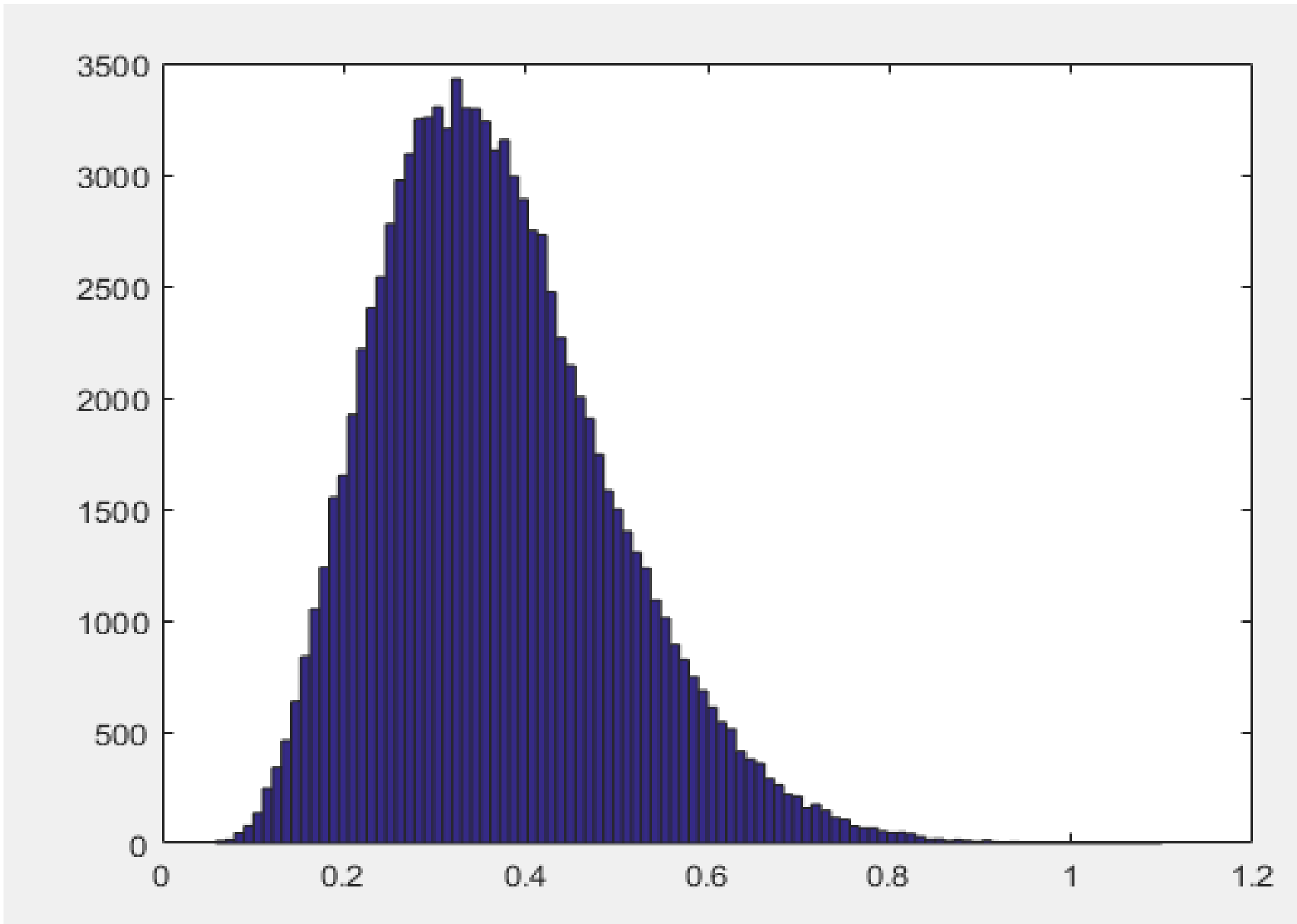


Relative Statistical Characterization of R-based DACs

INL histogram for 100,000 random implementations

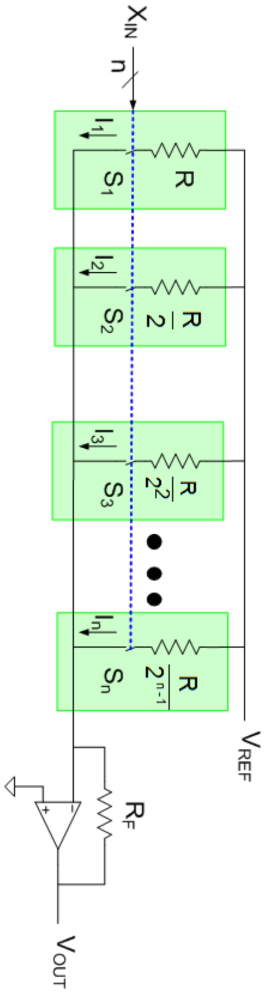


Binary Weighted DAC

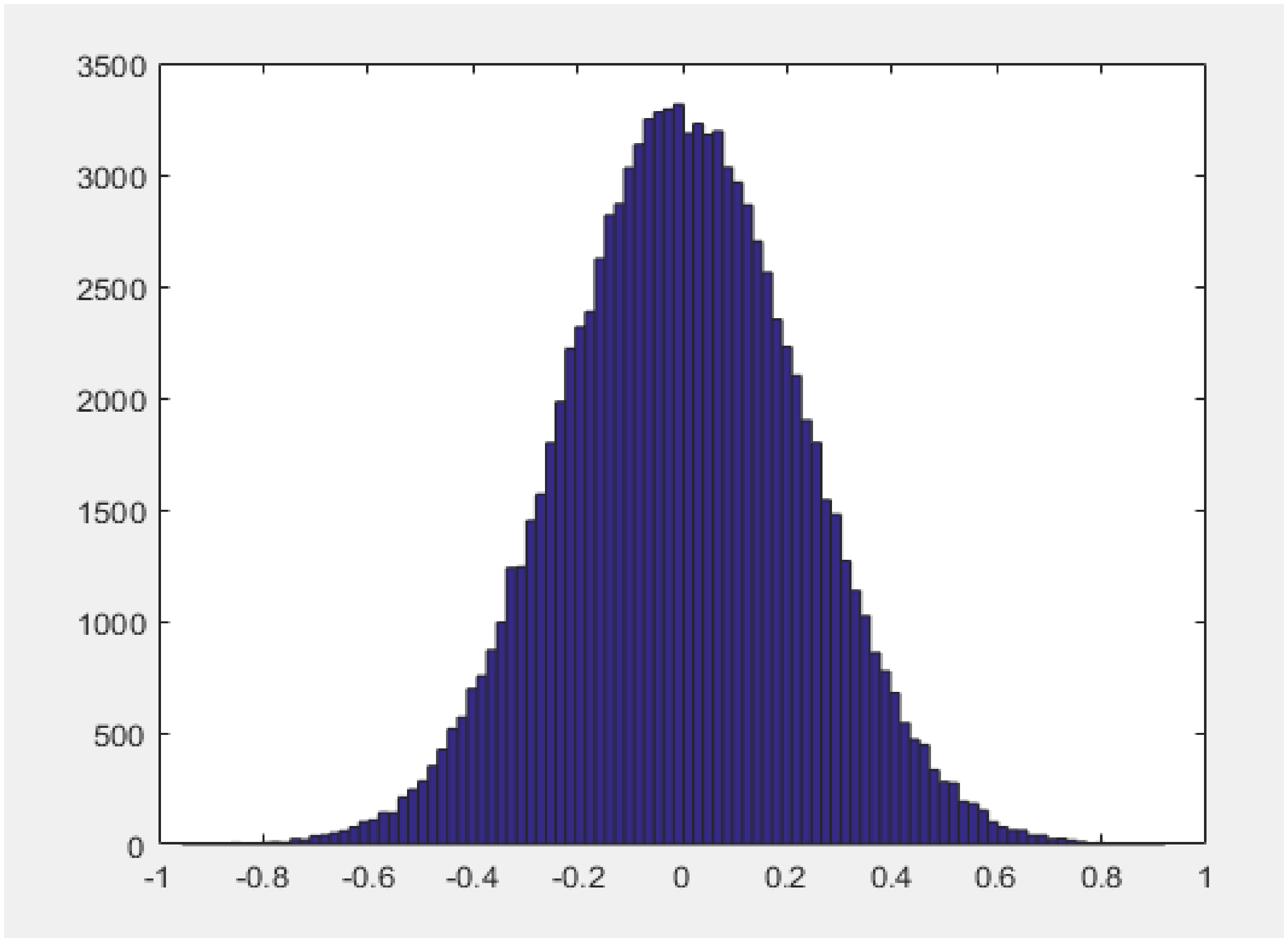


Relative Statistical Characterization of R-based DACs

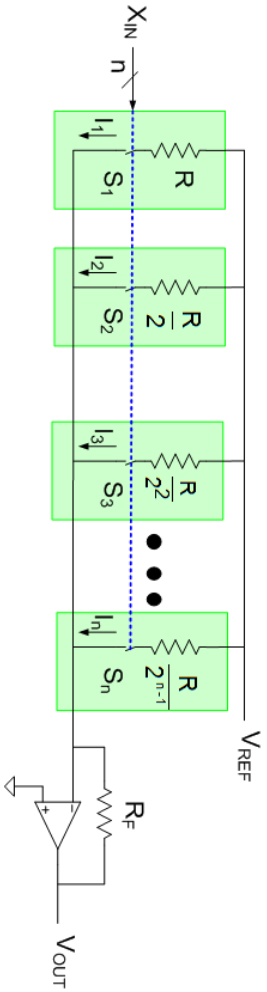
INL_{kMAX} histogram for 100,000 random implementations



Binary Weighted DAC

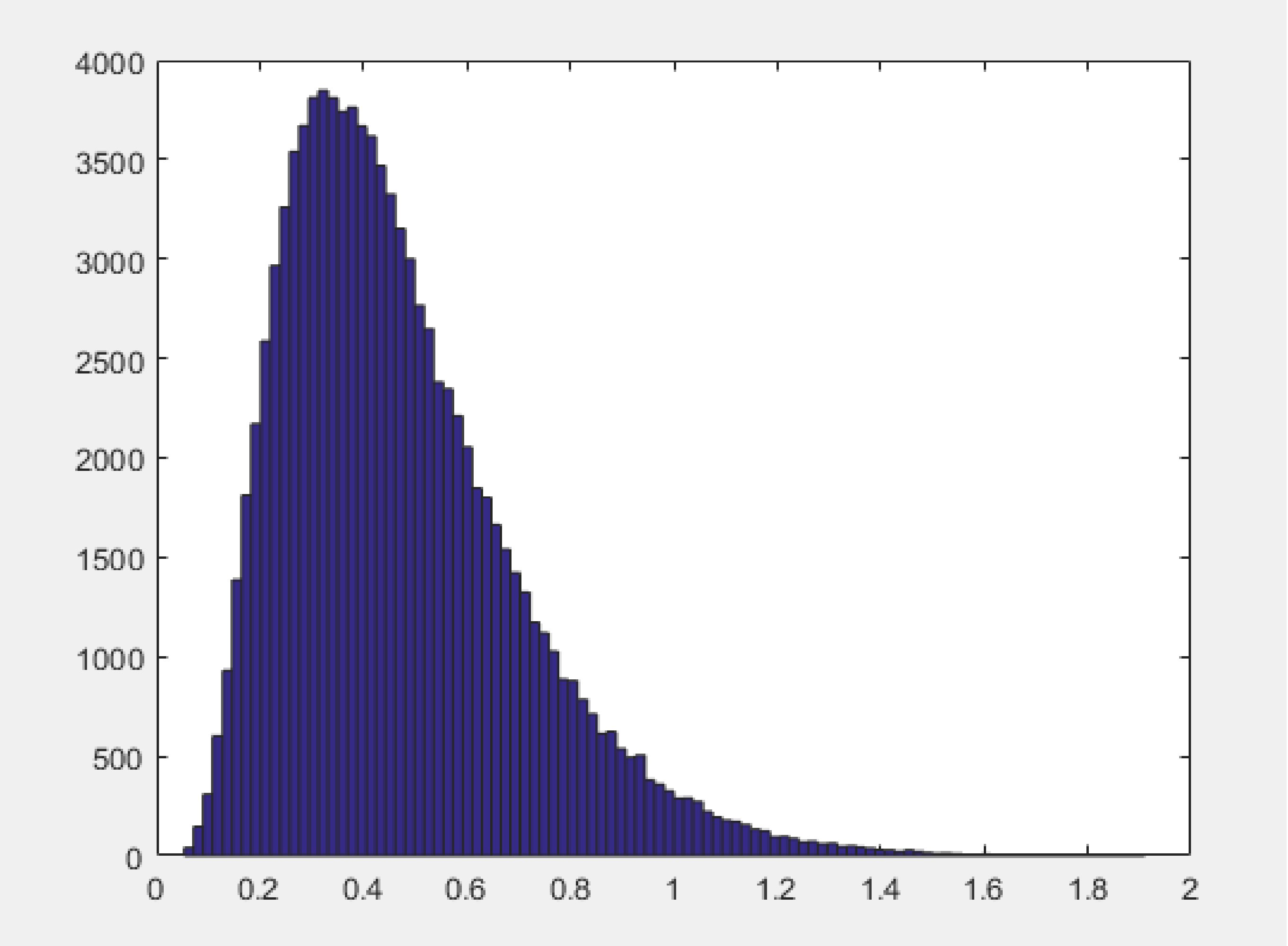


Relative Statistical Characterization of R-based DACs

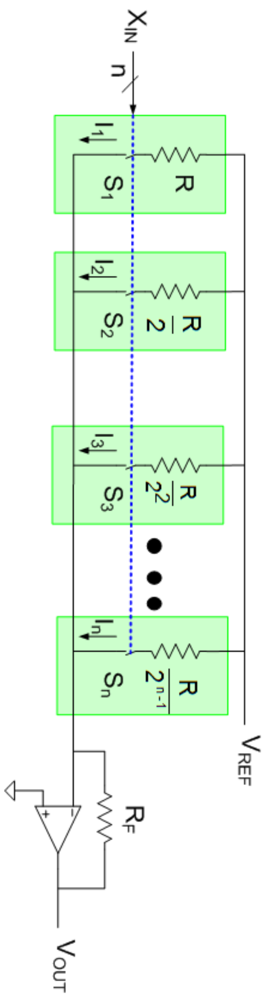


Binary Weighted DAC

DNL histogram for 100,000 random implementations



Relative Statistical Characterization of R-based DACs



Binary Weighted DAC

Summary

Resolution = 10

$A_{\rho R}$ = 0.02μm

R_{nom} = 1000

Area unit resistor=2μm^2

Resistor Sigma= 14.1421

INL_{mean} = 0.367LSB

INL_{sigma} = 0.128 LSB

INL_{kmax_mean} = 0.00013 LSB

INL_{kmax_sigma} = 0.226 LSB

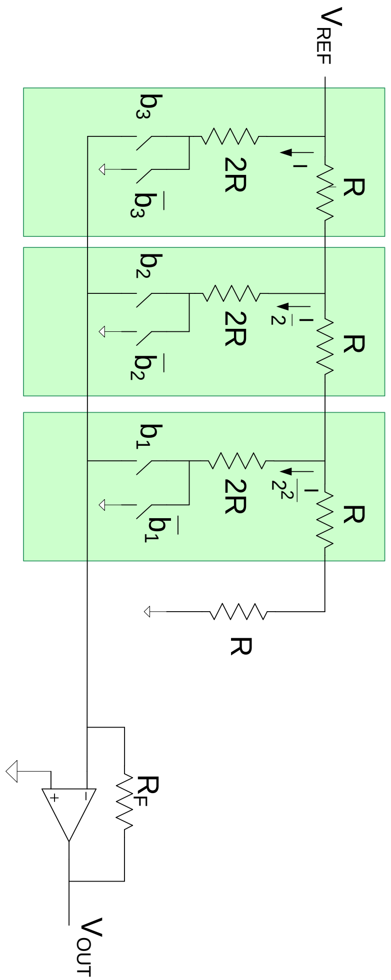
DNL_{mean} = 0.470 LSB

DNL_{sigma} = 0.228 LSB

INL_{target} = 0.500 LSB

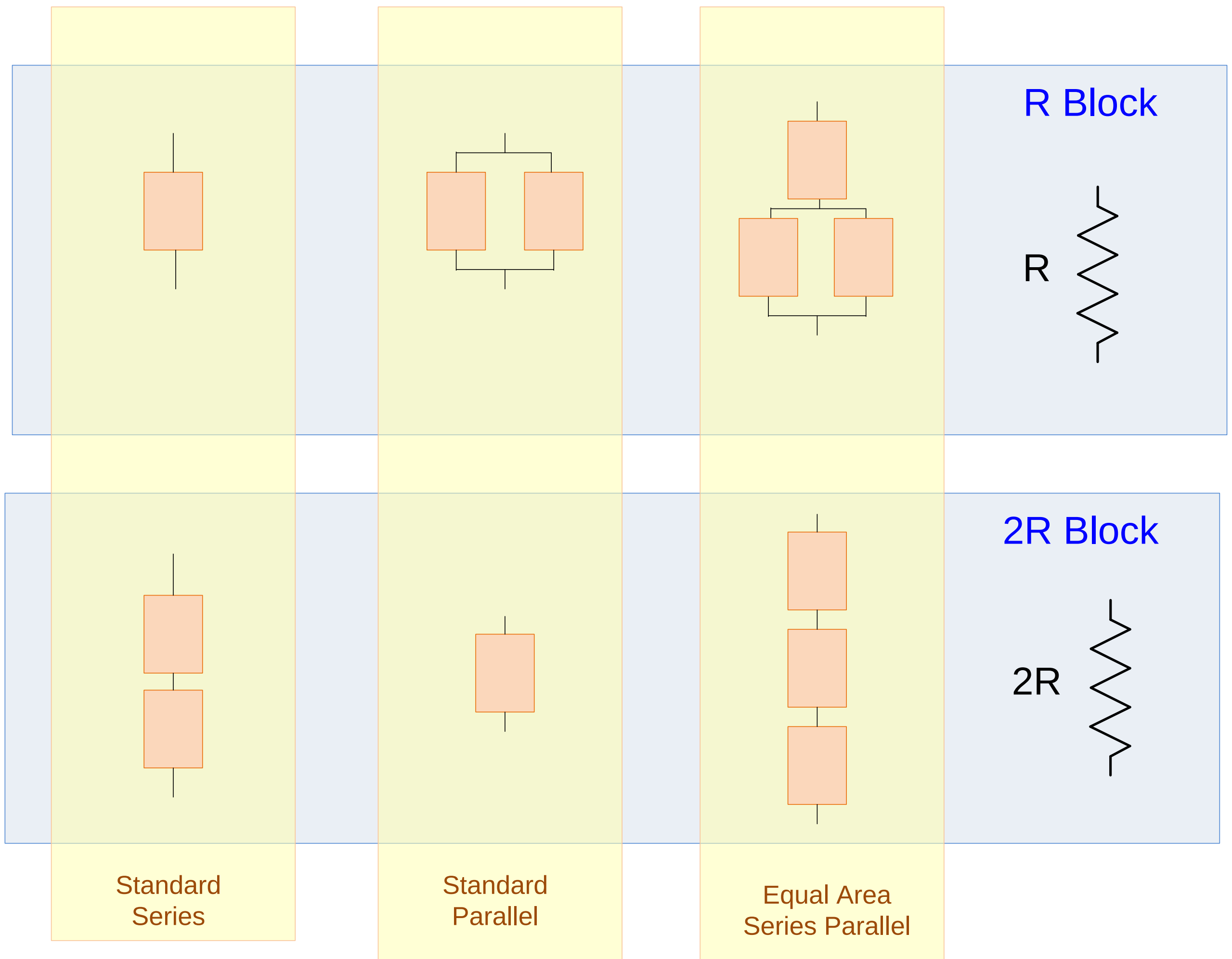
Yield (%) = 84.9

Relative Statistical Characterization of R-based DACs



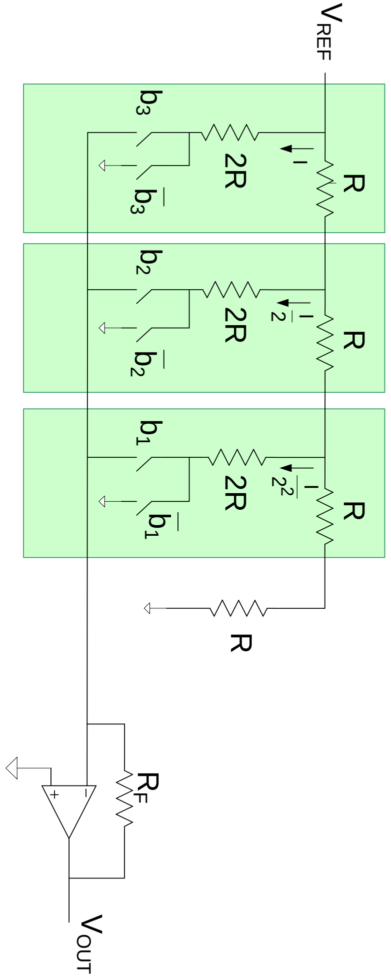
R-2R DAC

Popular Area Allocation Strategies

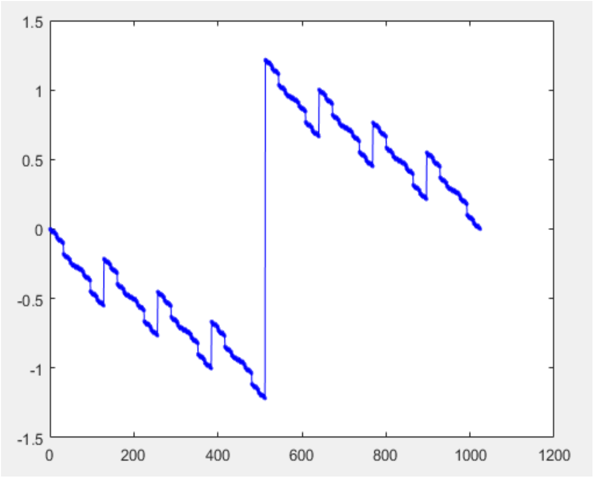


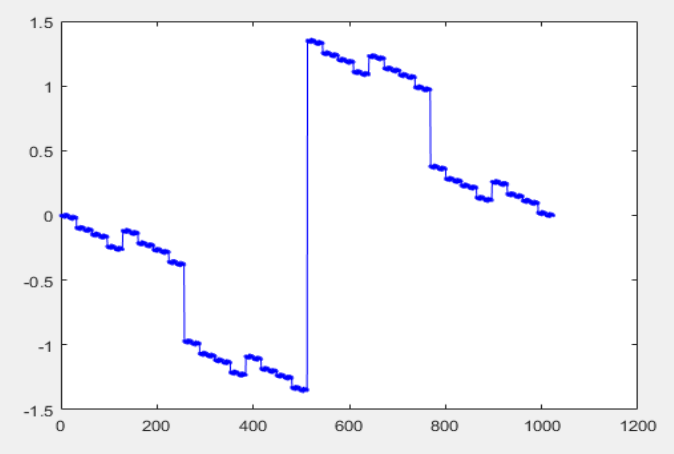
Relative Statistical Characterization of R-based DACs

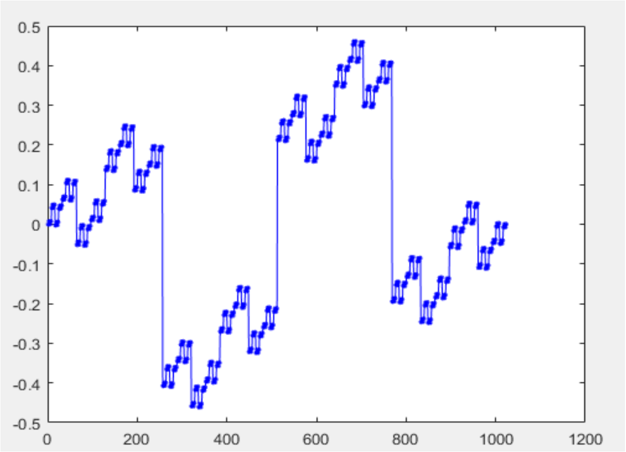
INL_k for four random standard series implementations

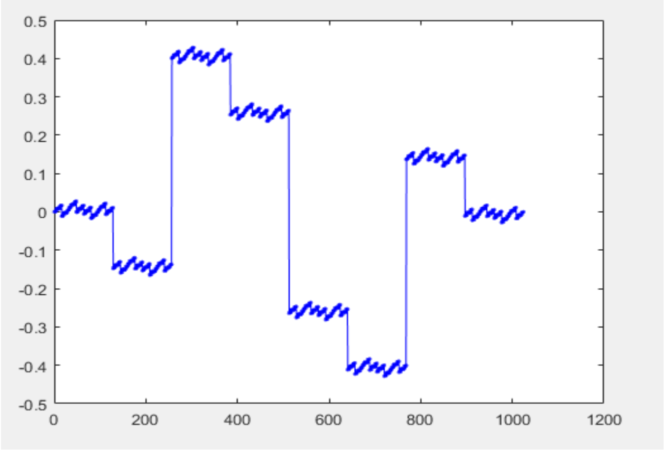


R-2R DAC



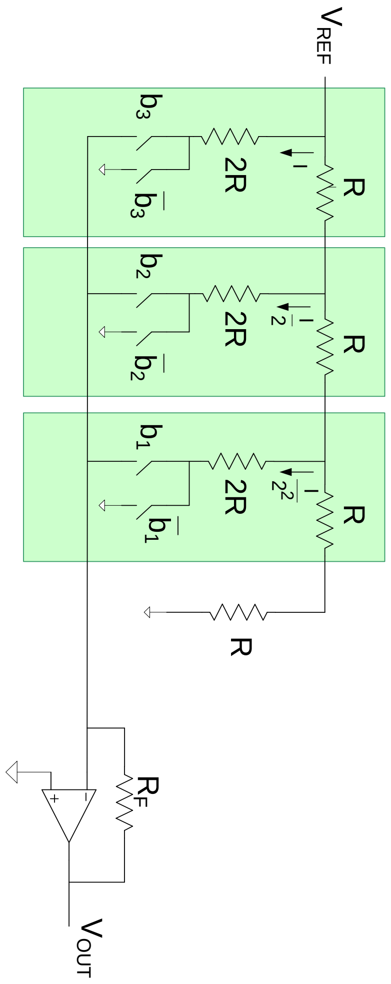




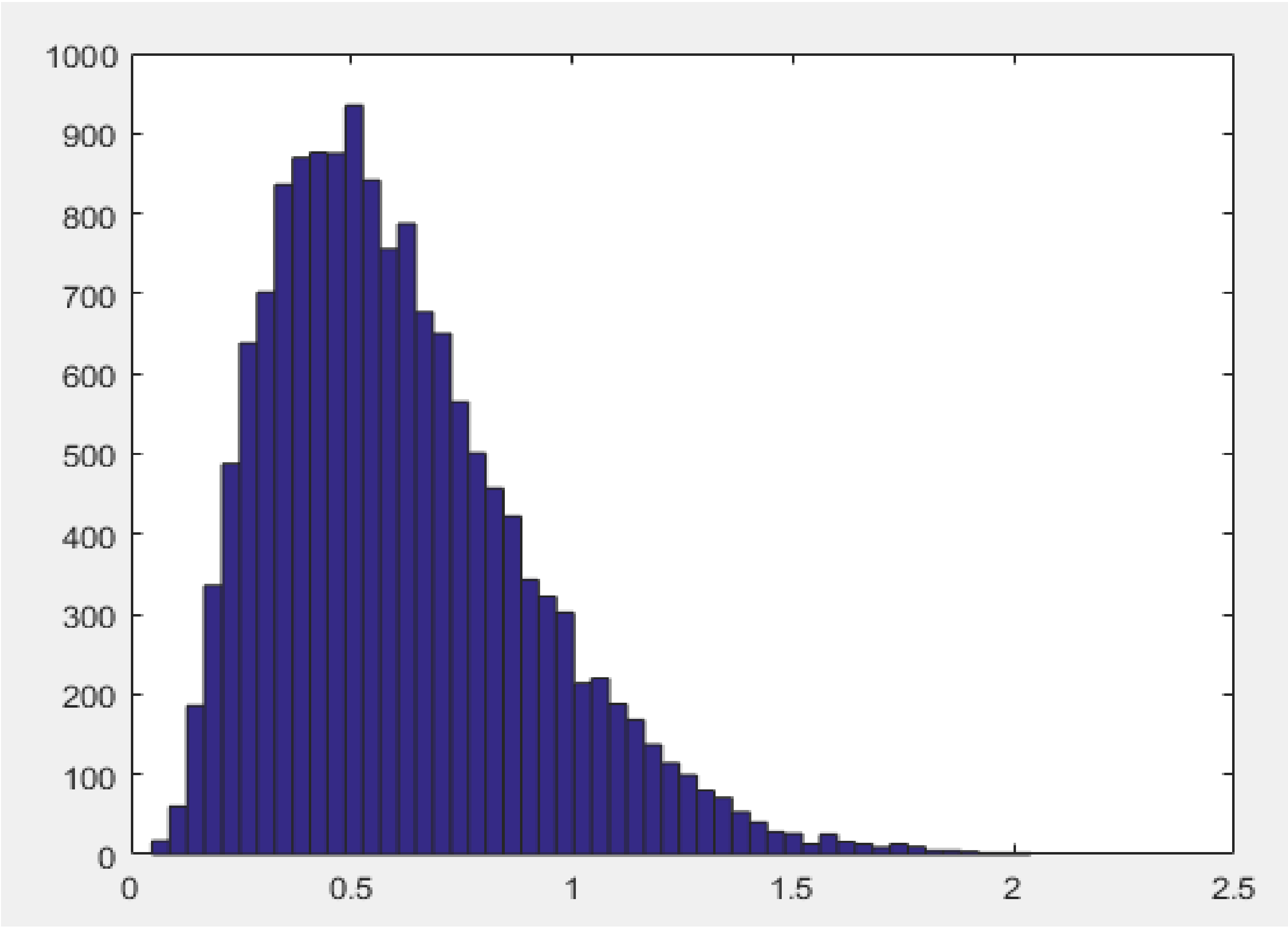


Relative Statistical Characterization of R-based DACs

INL histogram for 15,000 random implementations Standard Series

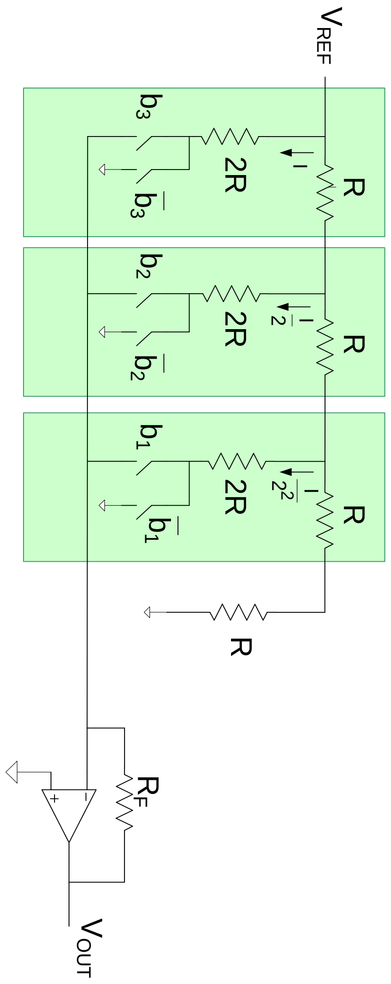


R-2R DAC

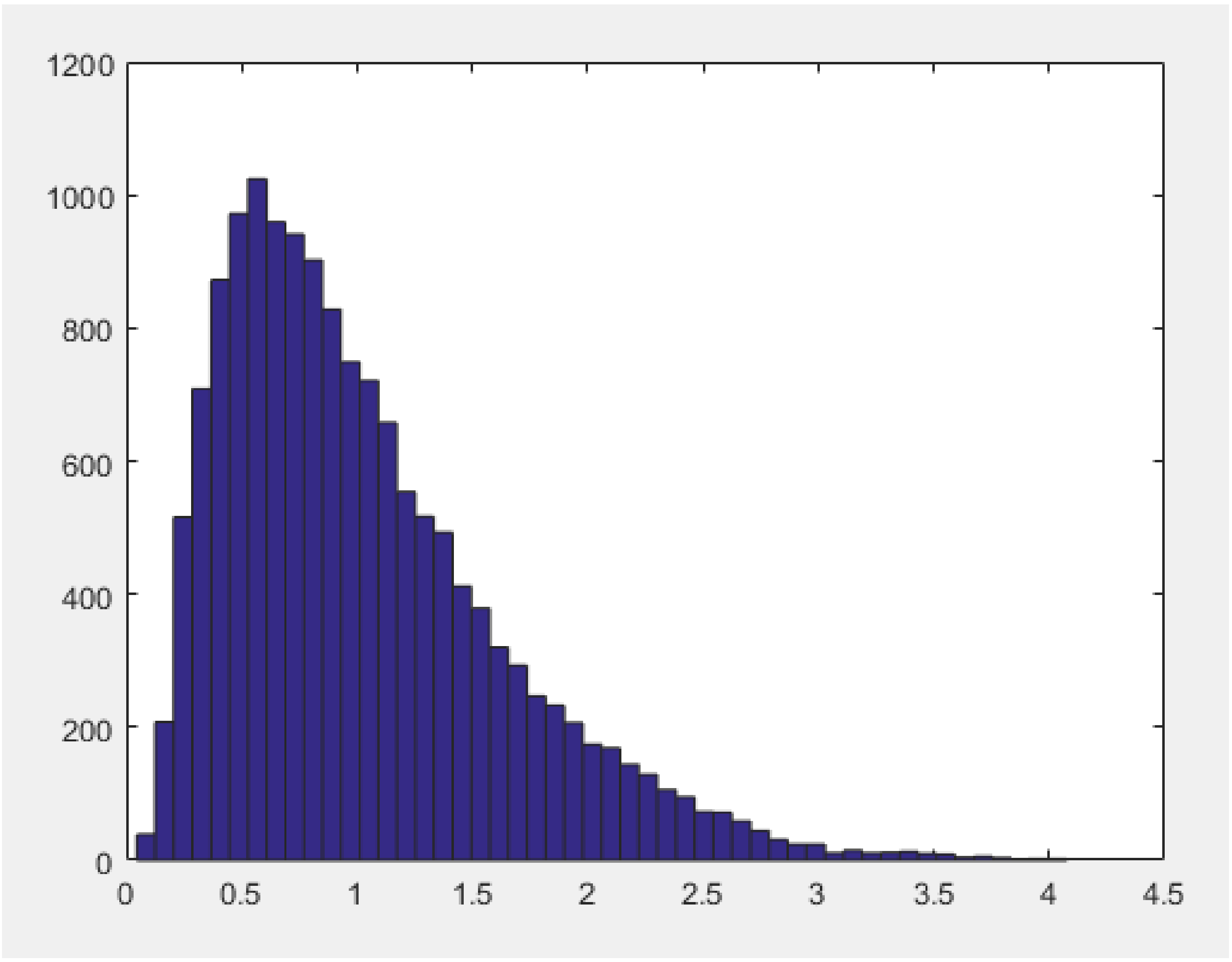


Relative Statistical Characterization of R-based DACs

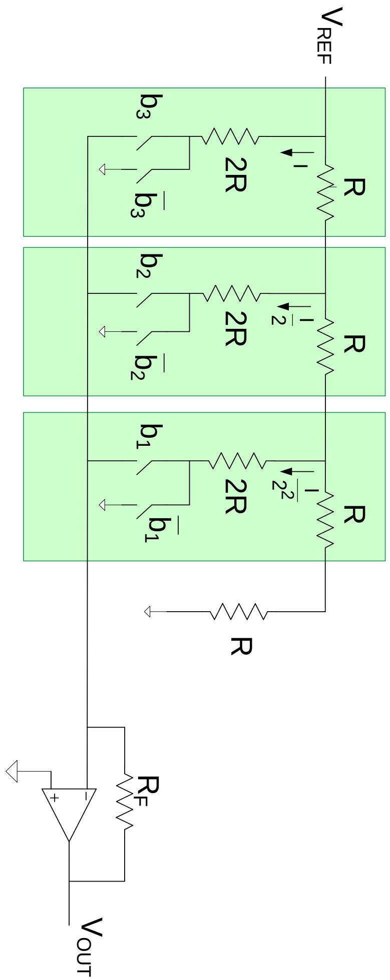
DNL histogram for 15,000 random implementations Standard Series



R-2R DAC



Relative Statistical Characterization of R-based DACs



R-2R DAC

Summary Standard Series

Resolution=10

$A_{\rho R}$=0.02 µm

Rnom = 1000

Base Res Area(um^2)=2

Res Sigma=14.1421

INL_{mean} = 0.609 LSB

INL_{sigma} = 0.295 LSB

DNL_{mean} = 1.021 LSB

DNL_{sigma} = 0.610 LSB

INL_{kmax_mean} = 0.00017 LSB

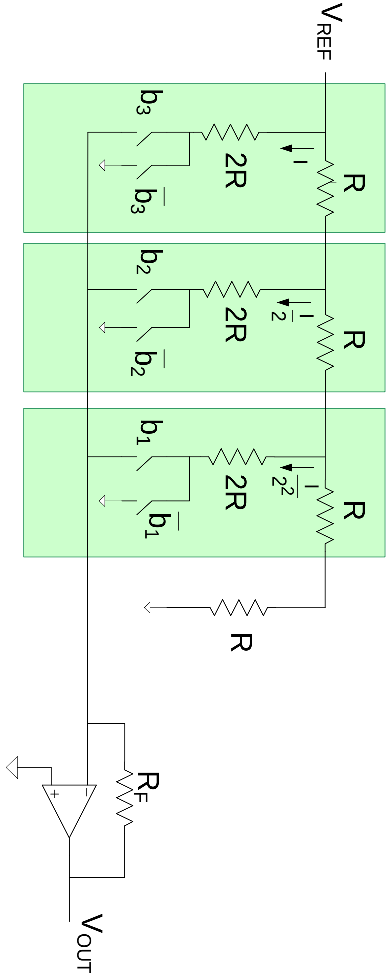
INL_{kmax_sigm}a = 0.566 LSB

Yield INL Bound=0.5 LSB

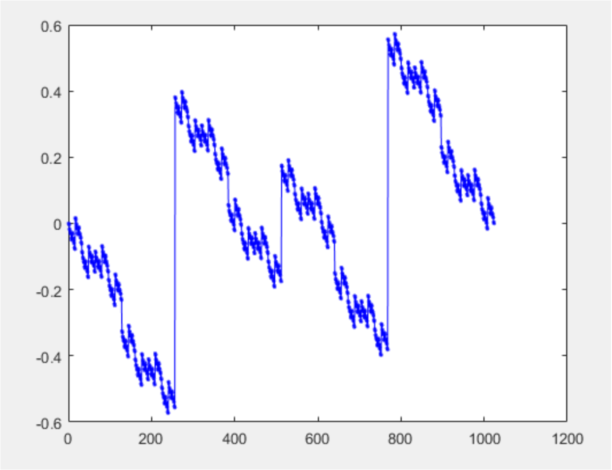
Yield= 41.4%

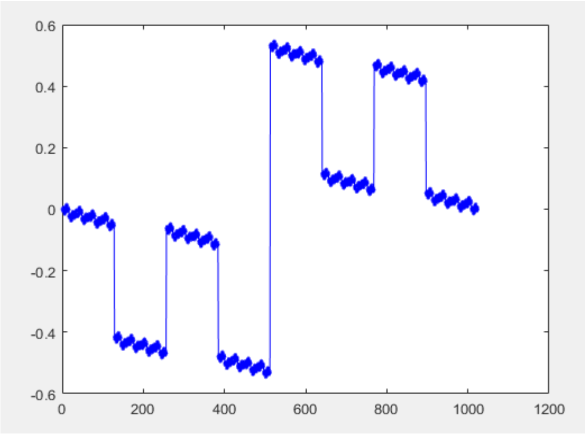
Relative Statistical Characterization of R-based DACs

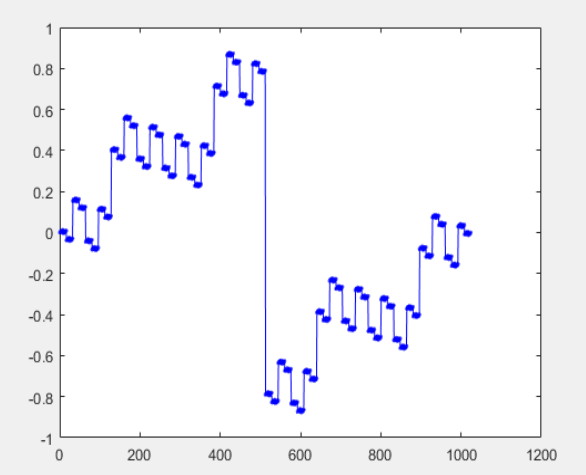
INL_k for four random standard parallel implementations

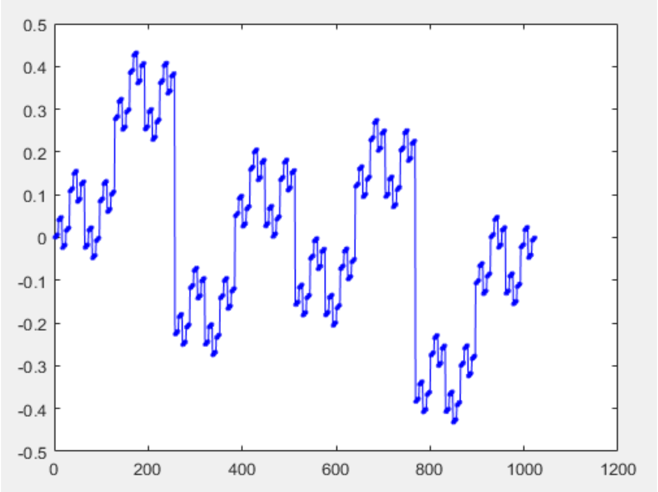


R-2R DAC



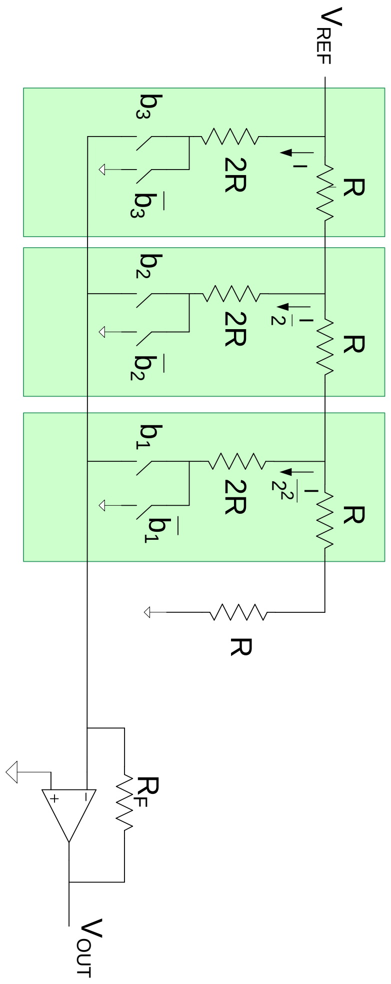




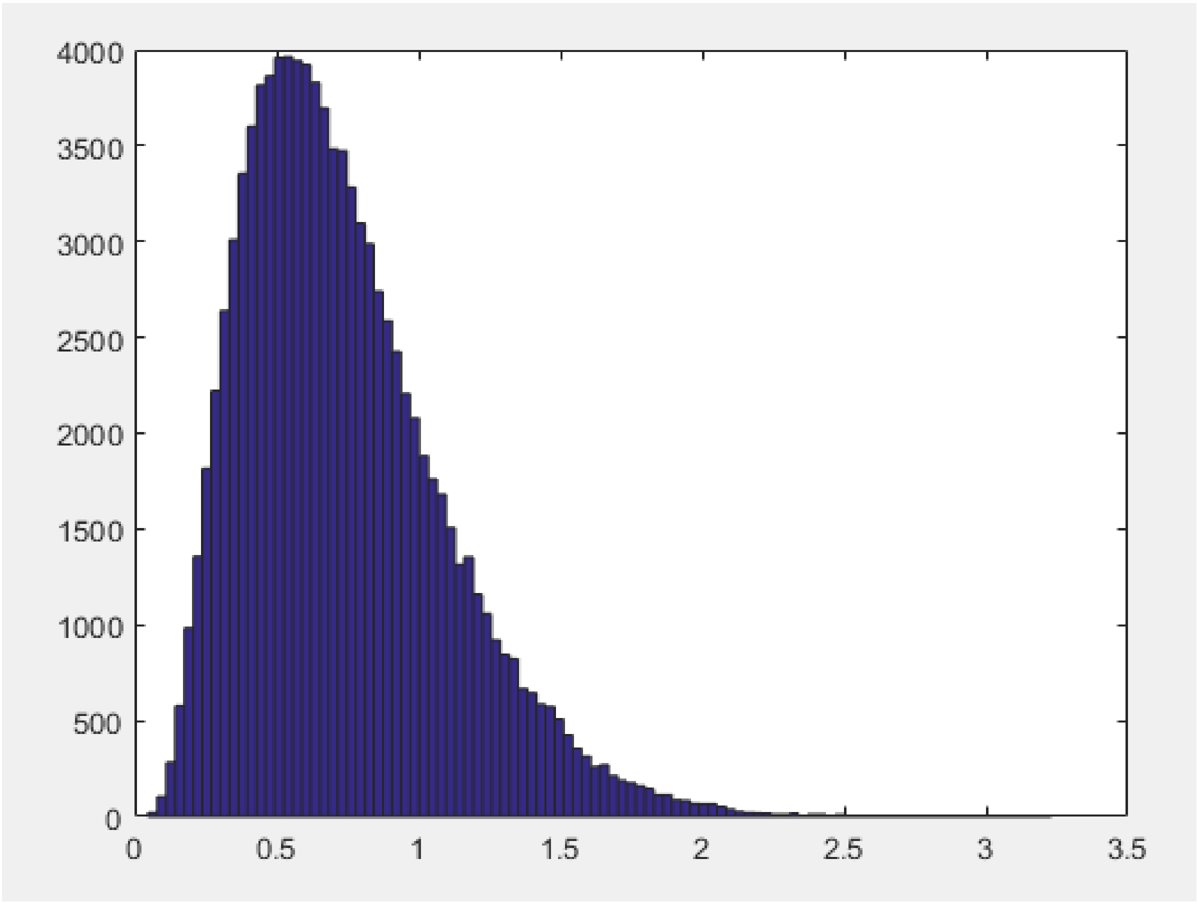


Relative Statistical Characterization of R-based DACs

INL histogram for 100,000 random implementations Standard Parallel

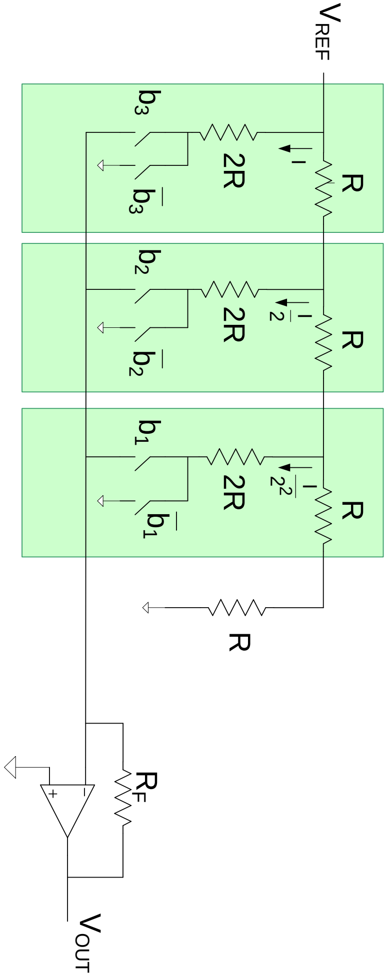


R-2R DAC

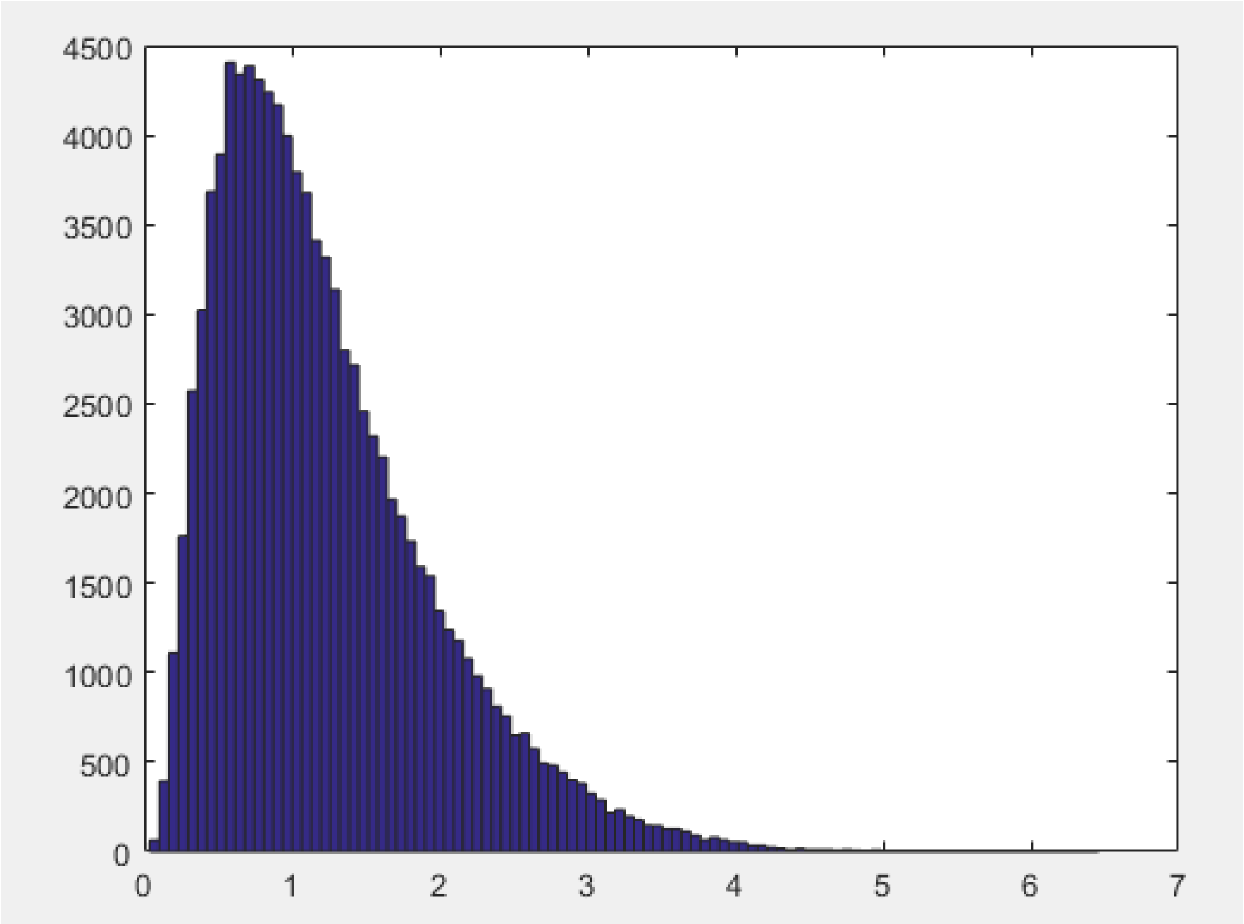


Relative Statistical Characterization of R-based DACs

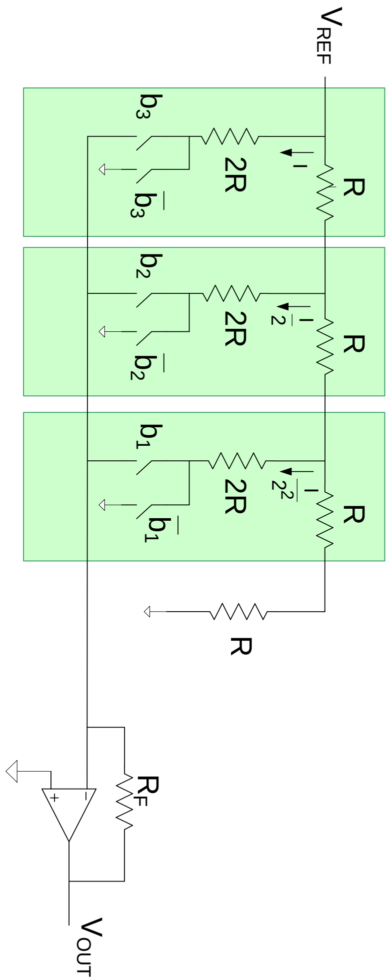
DNL histogram for 100,000 random implementations Standard Parallel



R-2R DAC



Relative Statistical Characterization of R-based DACs



R-2R DAC

Summary Standard Parallel

Resolution = 10

$A_{\rho R}$ = 0.02µm

R_{nom} = 1000

Base Resistor Area(um^2) = 2

Resistor Sigma= 14.1421

INL_{mean} = 0.737 LSB

INL_{sigma} = 0.357 LSB

INL_{kmax_mean} = 0.0045 LSB

INL_{kmax_sigma} = 0.680 LSB

DNL_{mean} = 1.225 LSB

DNL_{sigma} = 0.732 LSB

INL_{target} = 0.5 LS

Yield =28.5%

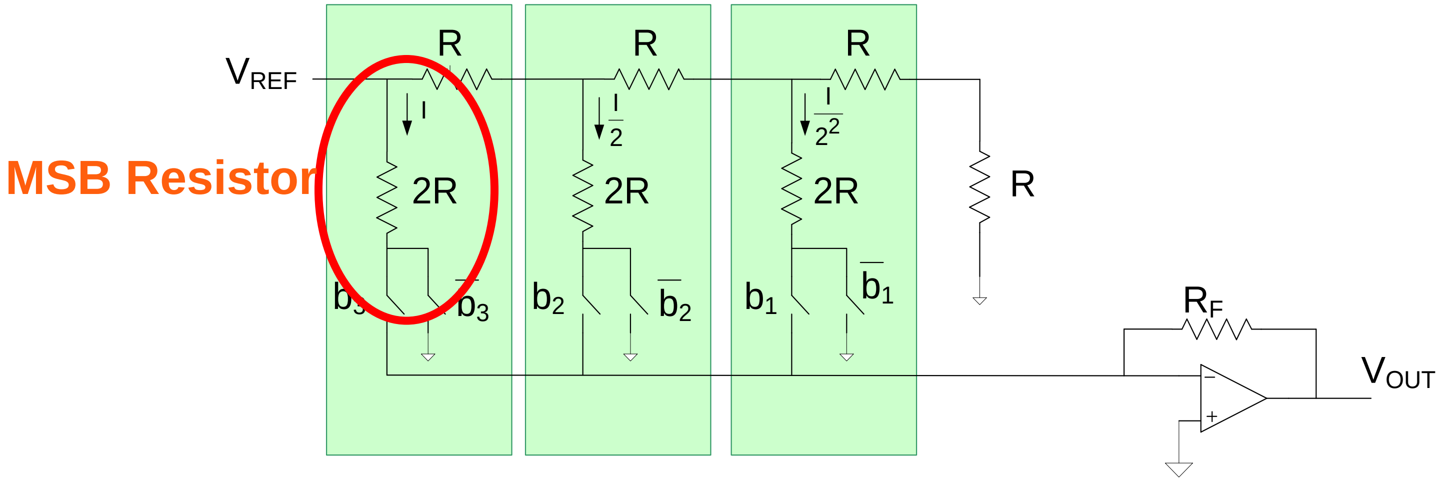
Why is the Standard Series yield significantly larger than the Standard Parallel?

Standard Parallel

Yield =28.5%

Standard Series

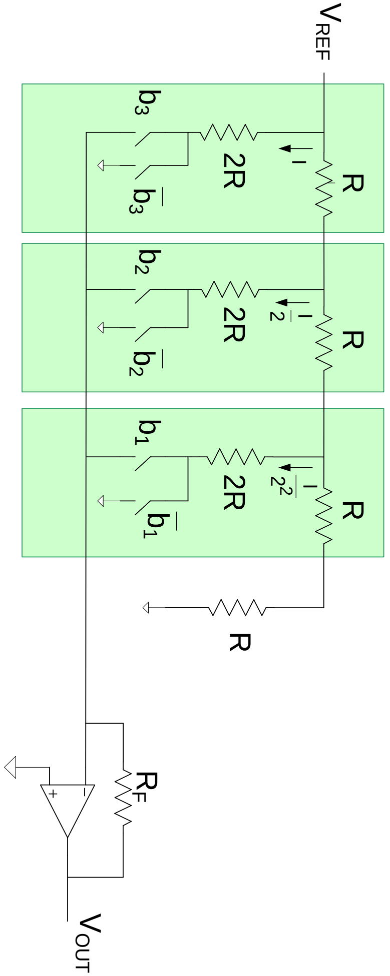
Yield= 41.4%



Each bit slice has the same area

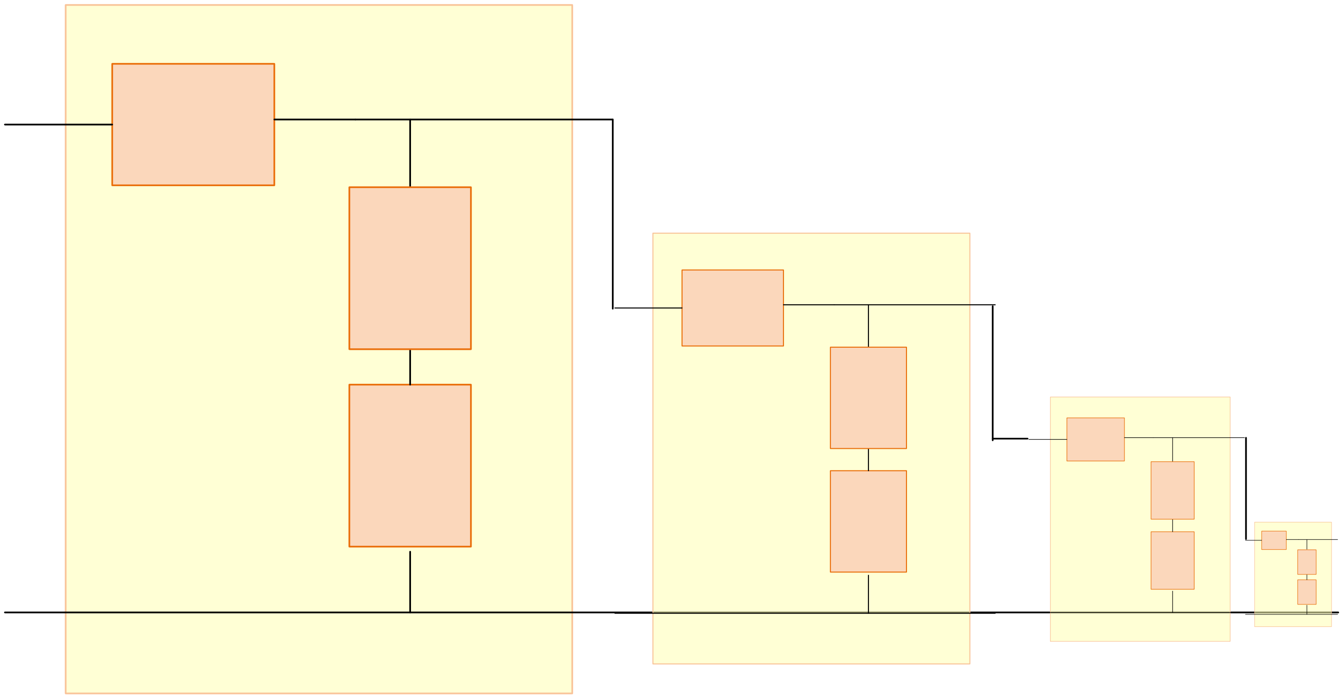
MSB resistor has higher percentage of area in Standard Series

Relative Statistical Characterization of R-based DACs



R-2R DAC

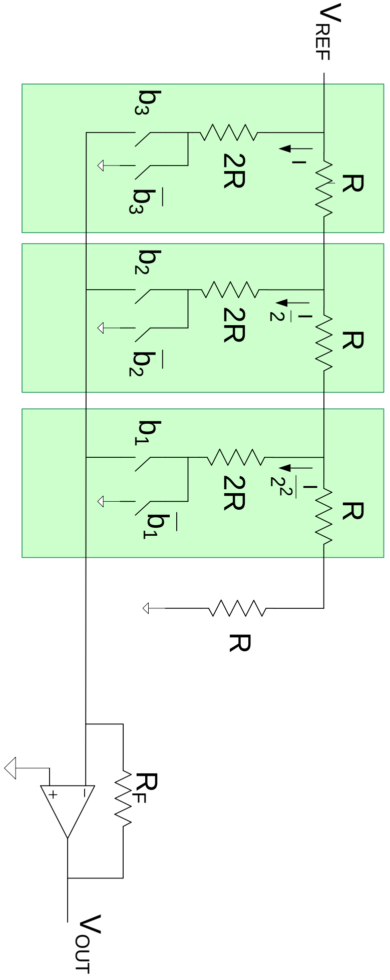
Standard Series Slice Area Scaled

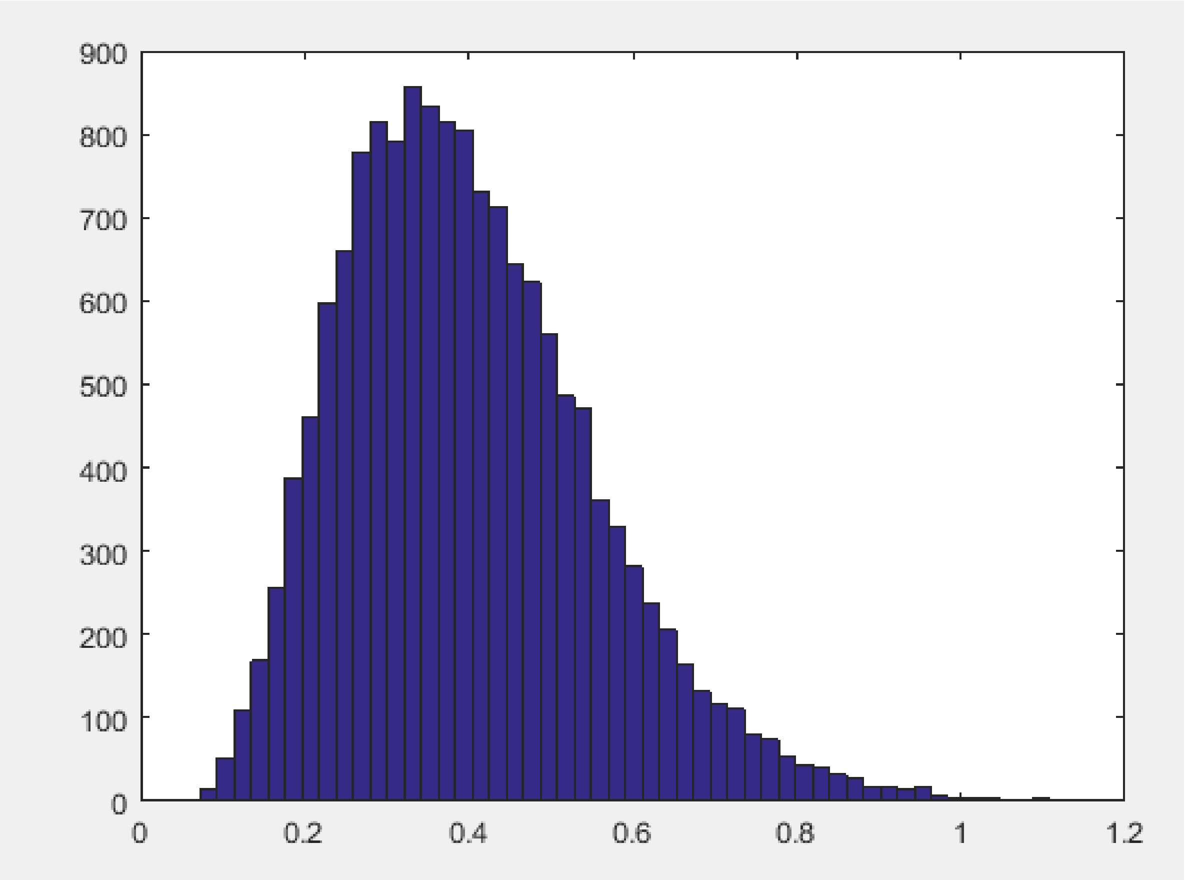


Relative Statistical Characterization of R-based DACs

DNL histogram for 15,000 random implementations Standard Series Area Scaled

Scaling Factor: 1.7



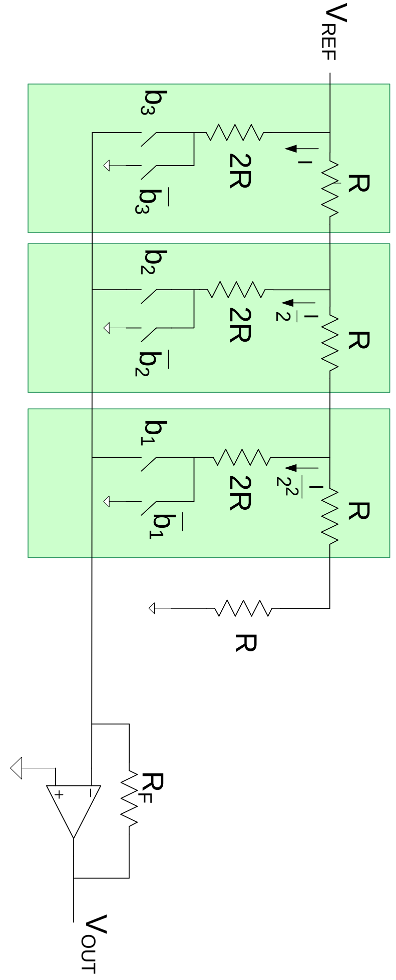


R-2R DAC

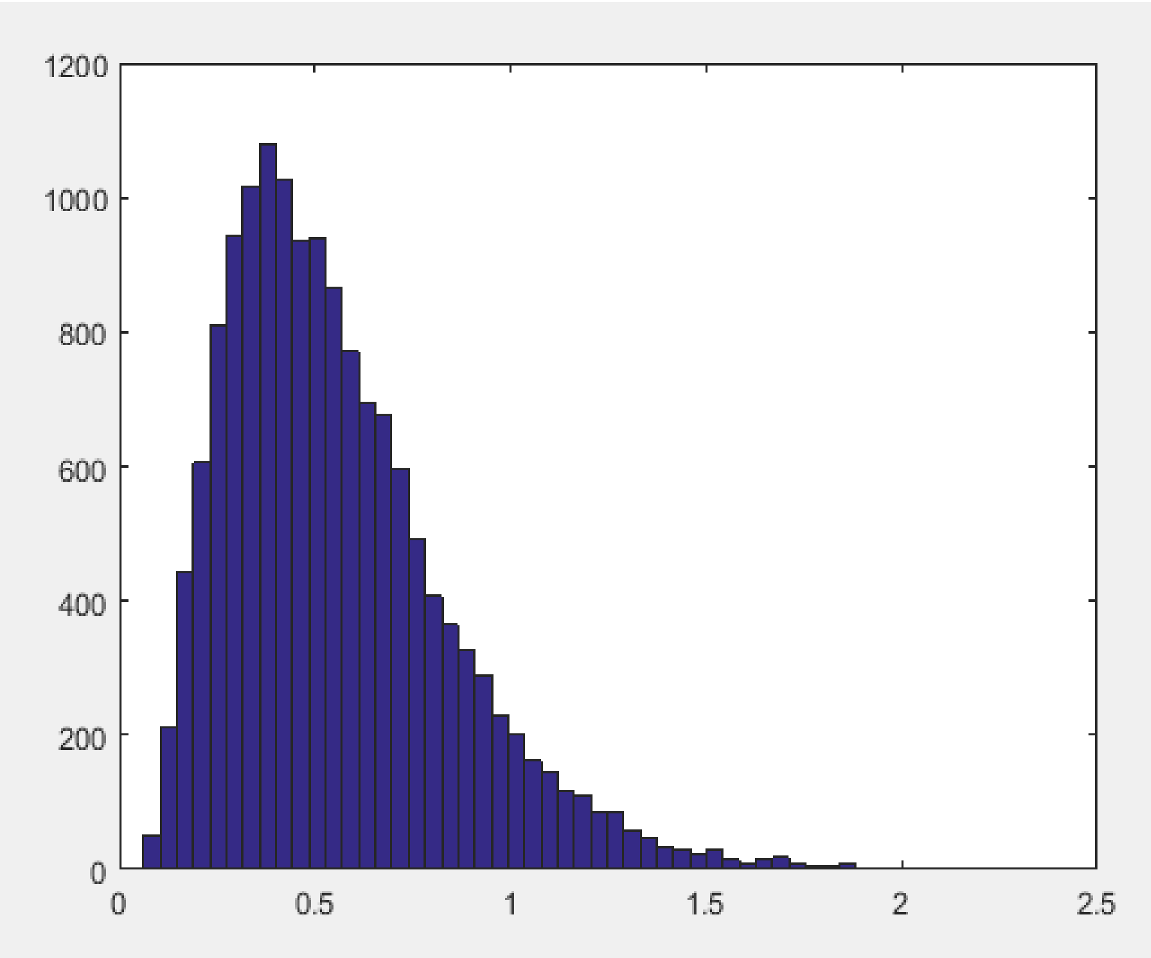
Relative Statistical Characterization of R-based DACs

INL histogram for 15,000 random implementations Standard Series Area Scaled

Scaling Factor: 1.7



R-2R DAC



Relative Statistical Characterization of R-based DACs

Resolution = 10
$A_{\rho R}$ = 0.02µm
R_{nom} = 1000
Total Area 2048 μm^2
Resistor Sigma= 14.1421
INL_{target} = 0.5 LSB
Yield =28.5%

Architecture	INL(LSB)		DNL(LSB)		INL Yield
	Mean	Sigma	Mean	Sigma	
String	0.385	0.118	0.049	0.0047	84.0
Binary Weighted	0.367	0.128	0.470	0.228	84.9
R-2R Series	0.609	0.295	1.021	0.610	41.4
R-2R Parallel	0.737	0.357	1.225	0.732	28.5
Slice Scaled (1.7) Series R-2R	0.399	0.153	0.556	0.286	76.4

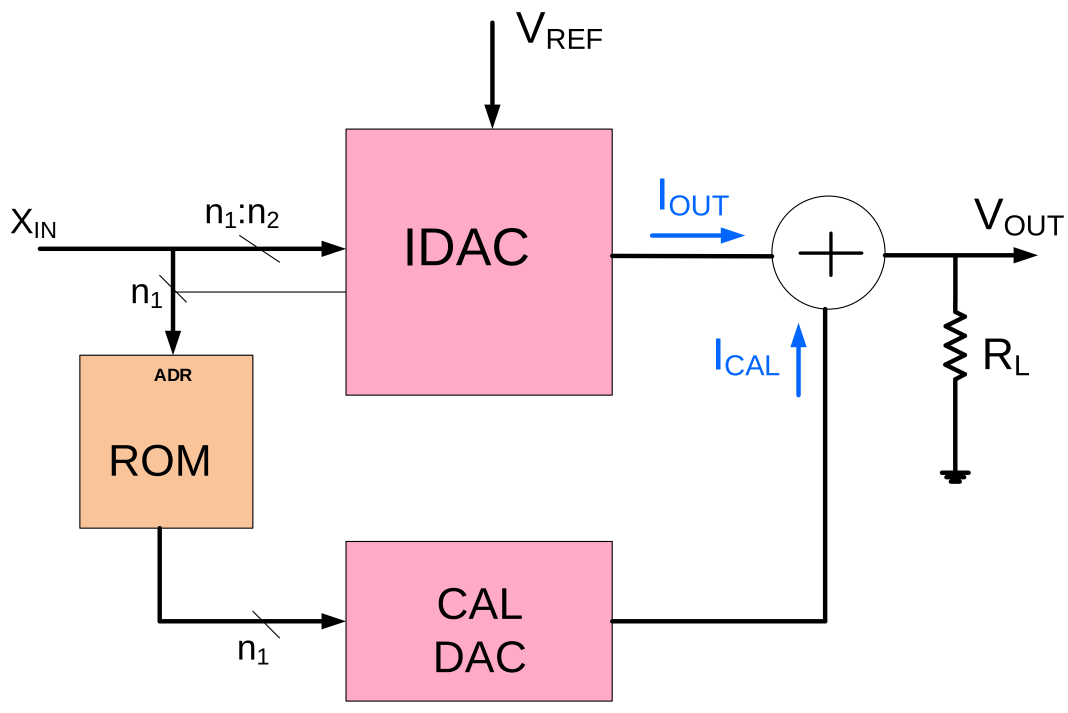
Calibration of DACs

- The area required to get acceptable performance of a DAC is often too large to be practical
- Large DAC area invariably increased power dissipation
- Large DAC area invariably limits speed of a DAC
- Calibration is often used to improve the linearity of a DAC
- Calibration requires area overhead but it is often less than the area overhead that is required to improve yield using area alone

$$\sigma_{\frac{X}{X_N}} = \frac{A_X}{\sqrt{A}}$$

- Benefits of using calibration are limited to the inherent noise in a DAC and calibration does not improve random noise (but can reduce quantization noise)

Calibration of DACs



- If CAL DAC is driven by appropriate information in RAM, it can correct for nonlinearities in IDAC
- Resolution of CAL DAC can be small if IDAC is modestly linear
- Code in ROM can be programmed at test or during production

- use a slow-speed ADC to determine actual output of IDAC & then add approp. output from CALDAC to obtain desired current

Dramatic Reduction Potential in Area for Higher-Resolution DACs

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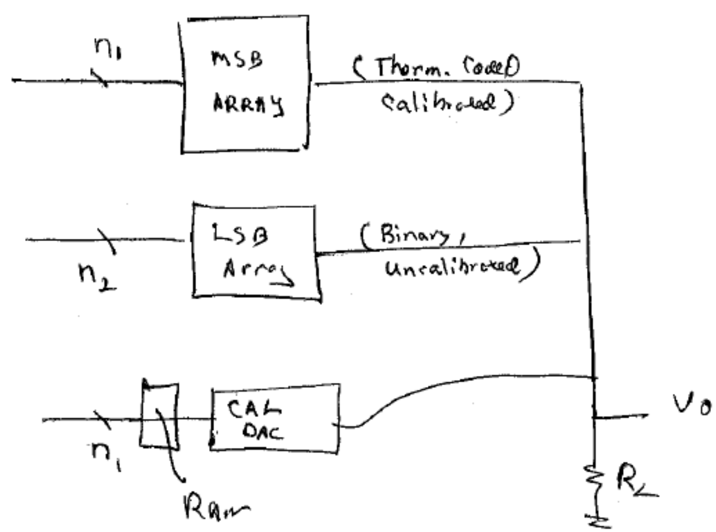
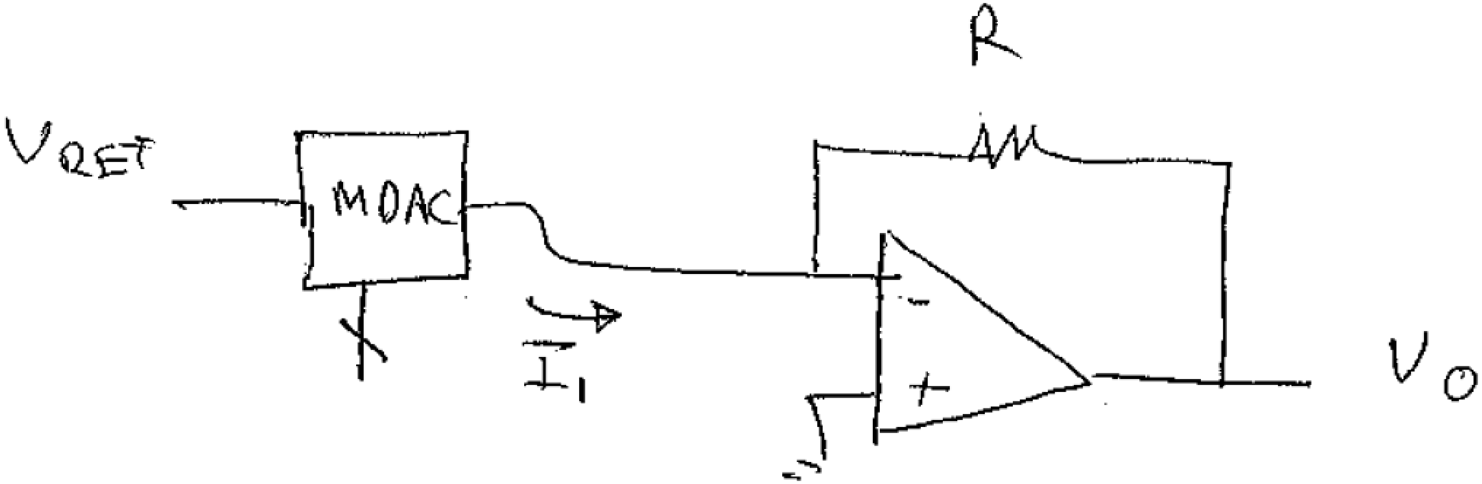


Higher-resolution DACs make extensive use of calibration or self-calibration

- Calibration corrects for nonlinearities (either discontinuities or smooth nonlinearities)
- Better high frequency performance
- Smaller die area
- Lower power dissipation
- Often more practical to calibrate for combined effects of all nonlinearities rather than correct the source of individual nonlinearities

Recall the MDAC



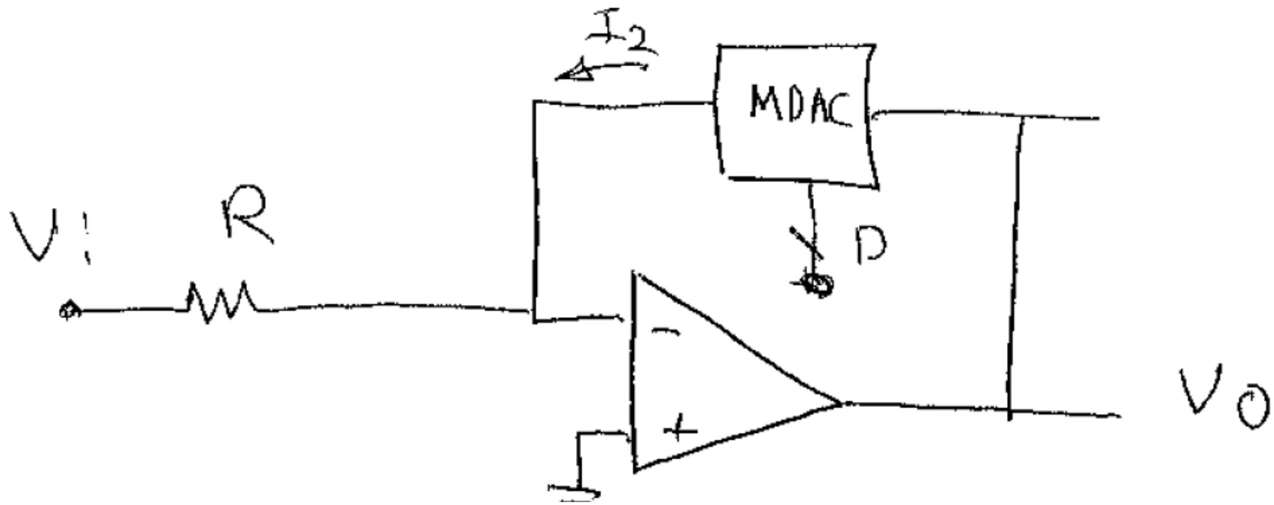
$$I_1 = (D\,V_{REF})(K)$$

$$V_O = -I_1 R$$

$$V_O = -RKD\,V_{REF}$$

$$= D\,[-RK]\,V_{REF}$$

Dividing DACs



$$I_2 = V_o D k$$

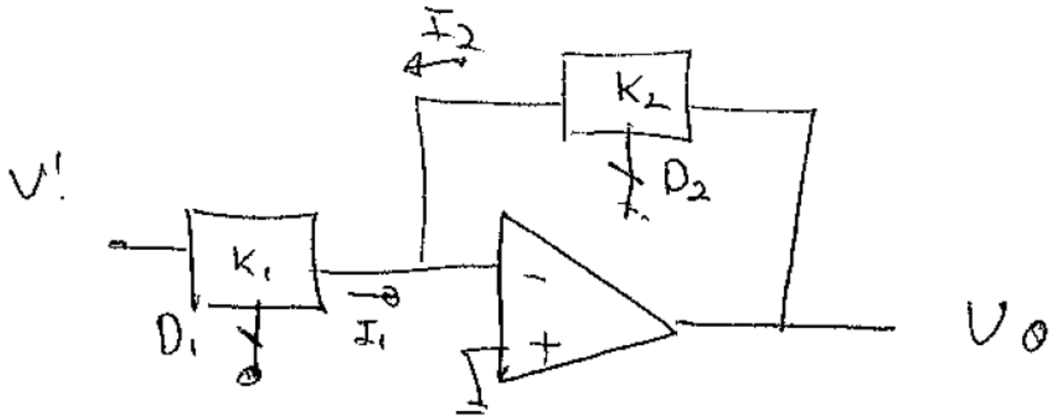
$$V_i = -I_2 R$$

$$V_i = -V_o D k R$$

$$V_o = + V_i \left(\frac{1}{D}\right)\left(\frac{-1}{kR}\right)$$

could call this D DAC

Multiplying and Dividing DACs



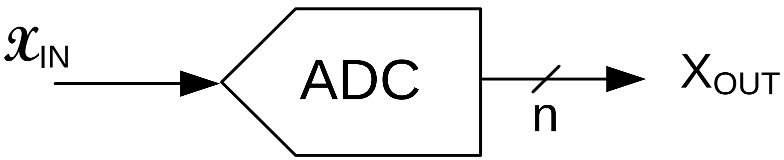
$$\begin{cases} I_1 = K_1 V_i D_1 \\ I_2 = V_0 D_2 K_2 \end{cases}$$

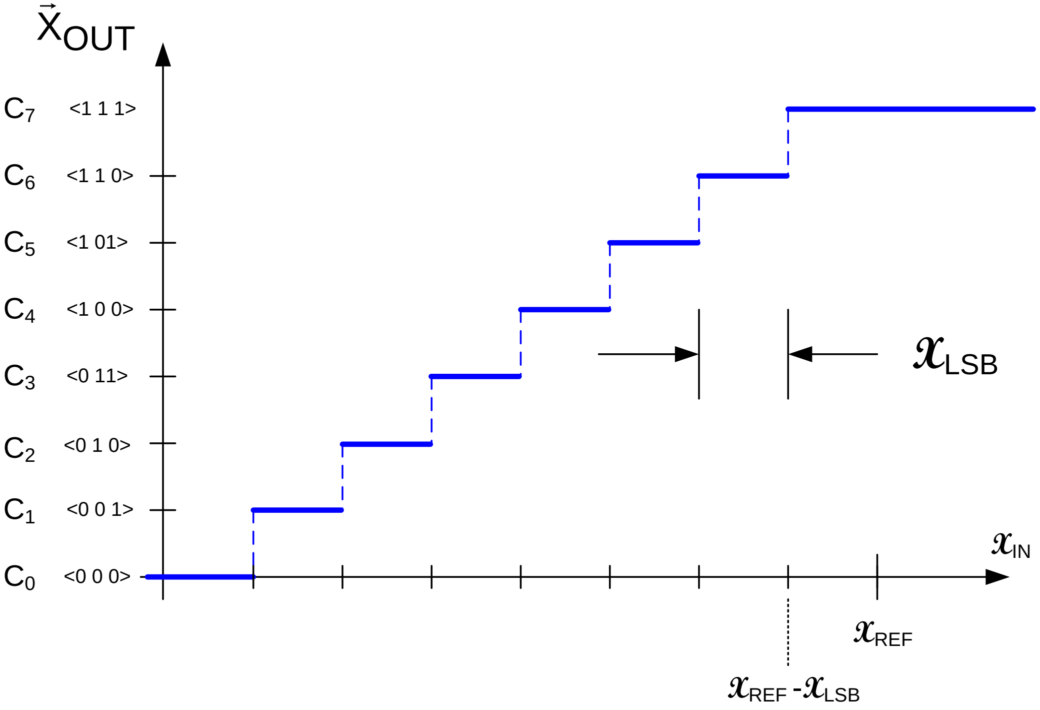
$$\therefore \quad V_0 = \frac{D_1}{D_2}\left[-\frac{k_1 V_i}{K_2}\right]$$

Can create various nonlinear relationships with MDACs and Op Amps

ADC Design

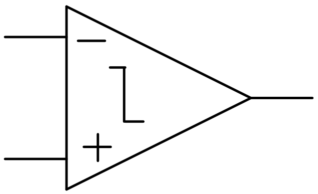
Analog to Digital Converters

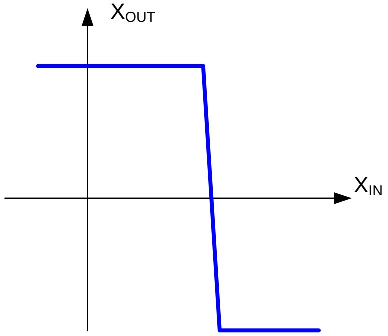




Analog to Digital Converters

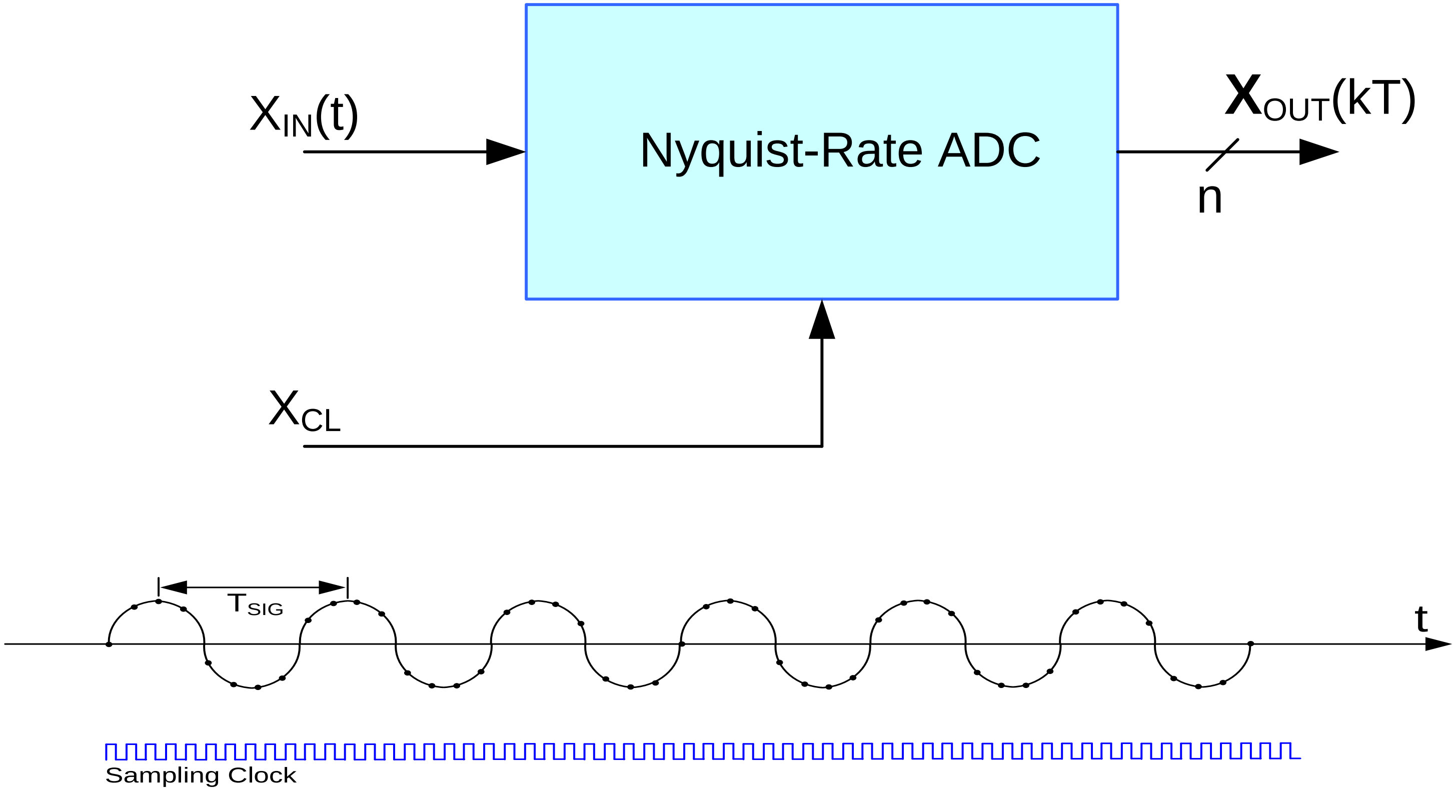
The conversion from analog to digital in ALL ADCs is done with comparators



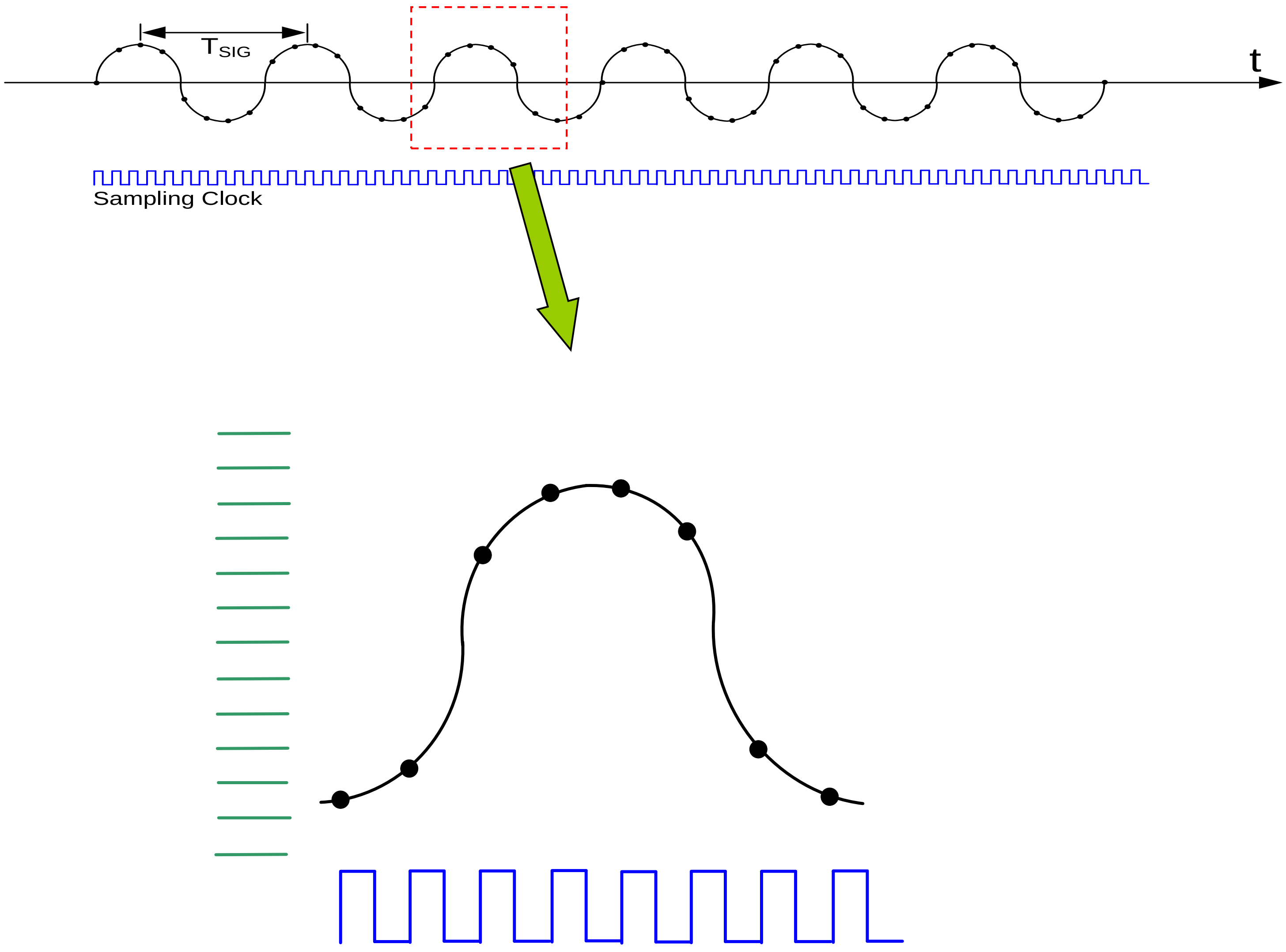


ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

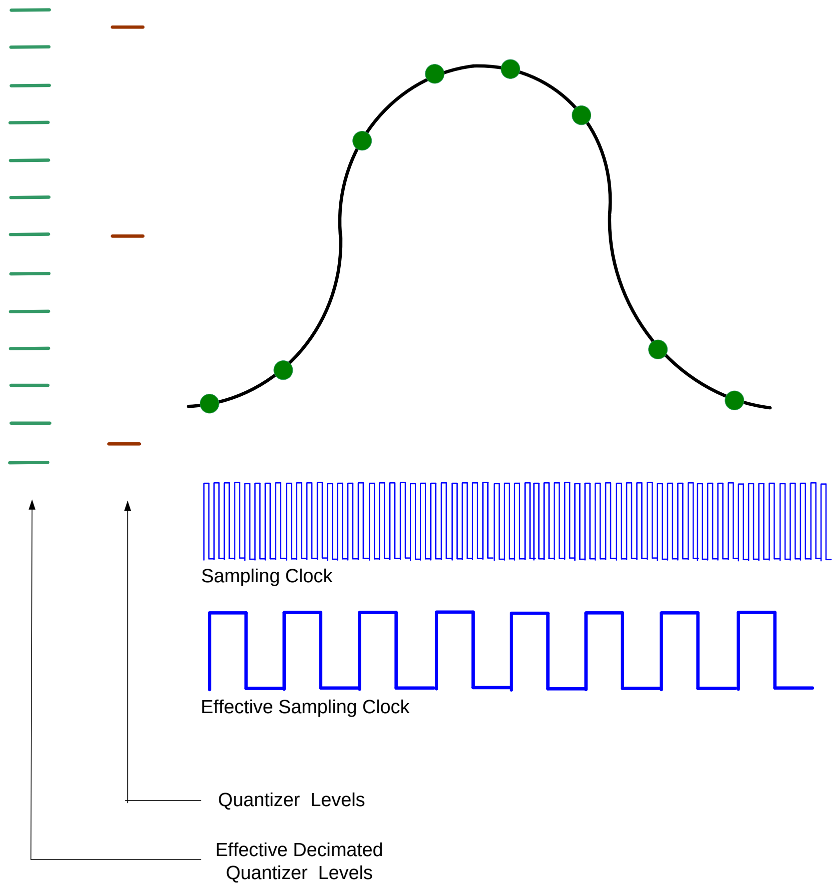
Nyquist Rate



Nyquist Rate

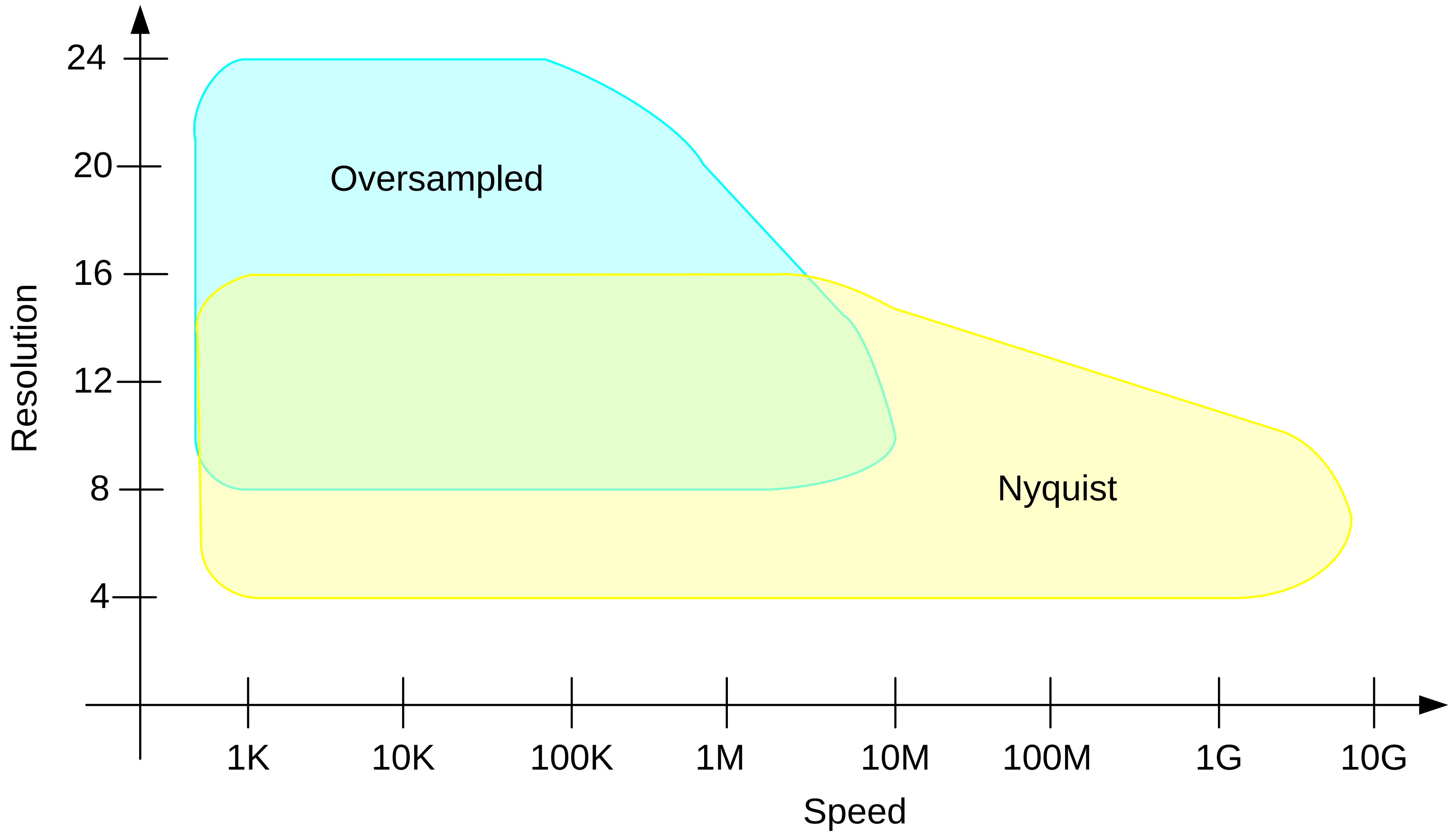


Over-Sampled



Over-sampling ratios of 128:1 or 64:1 are common
Dramatic reduction in quantization noise effects
Limited to relatively low frequencies

Data Converter Type Chart



ADC Types

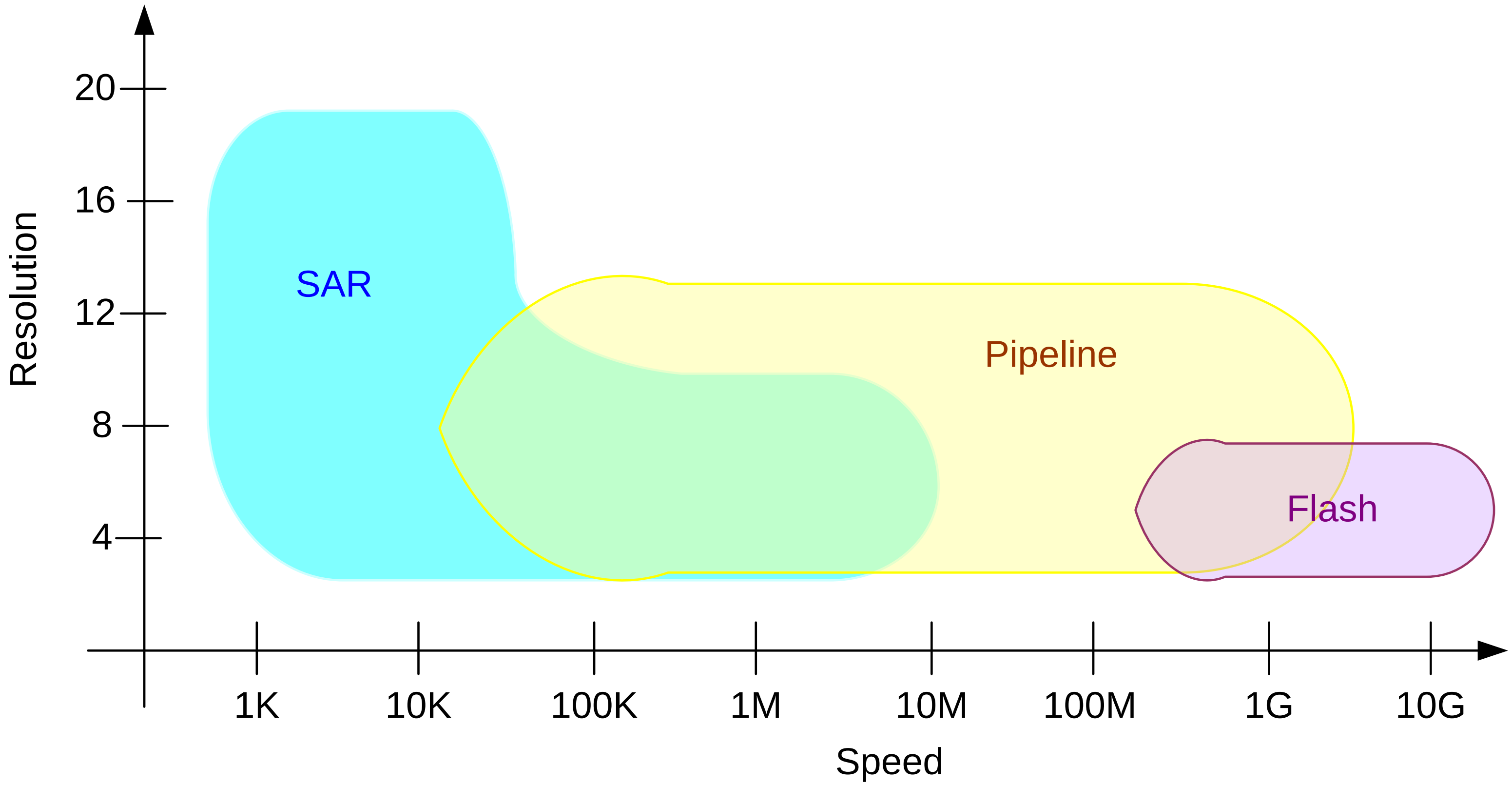
Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Nyqyist Rate Usage Structures



Flash is the least used as a stand-alone structure but widely used as a subcomponent in SAR and Pipelined Structures

ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

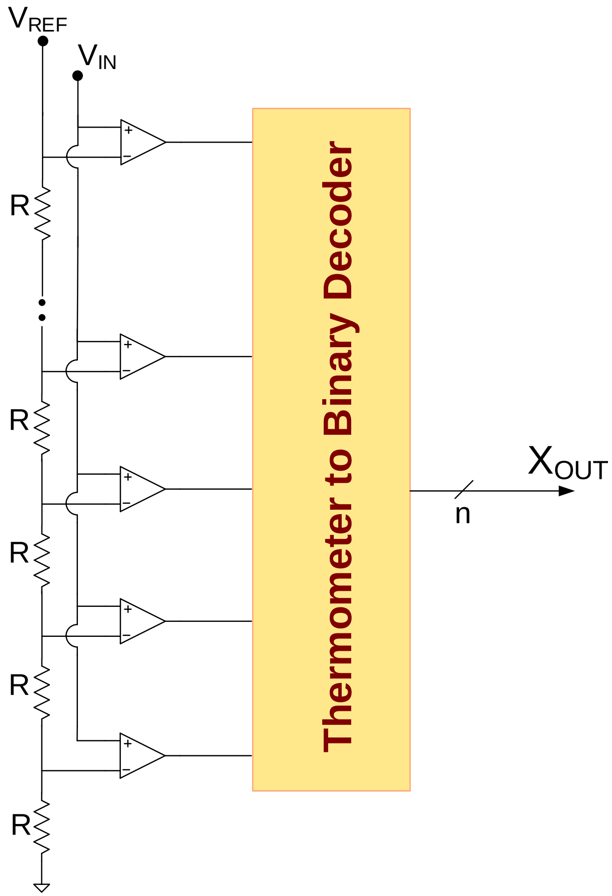
Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

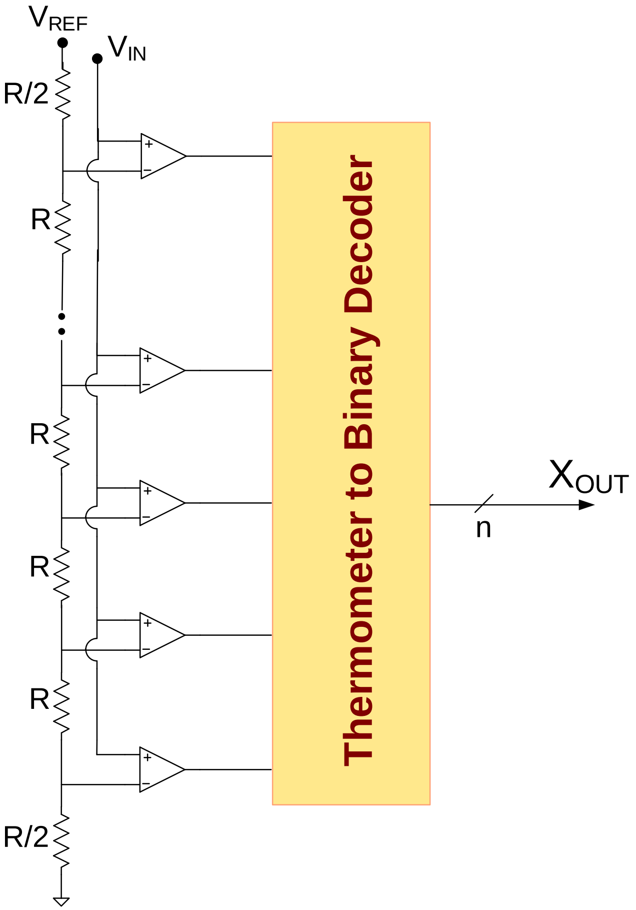
All have comparable conversion rates

Basic approach in all is very similar

Flash ADC

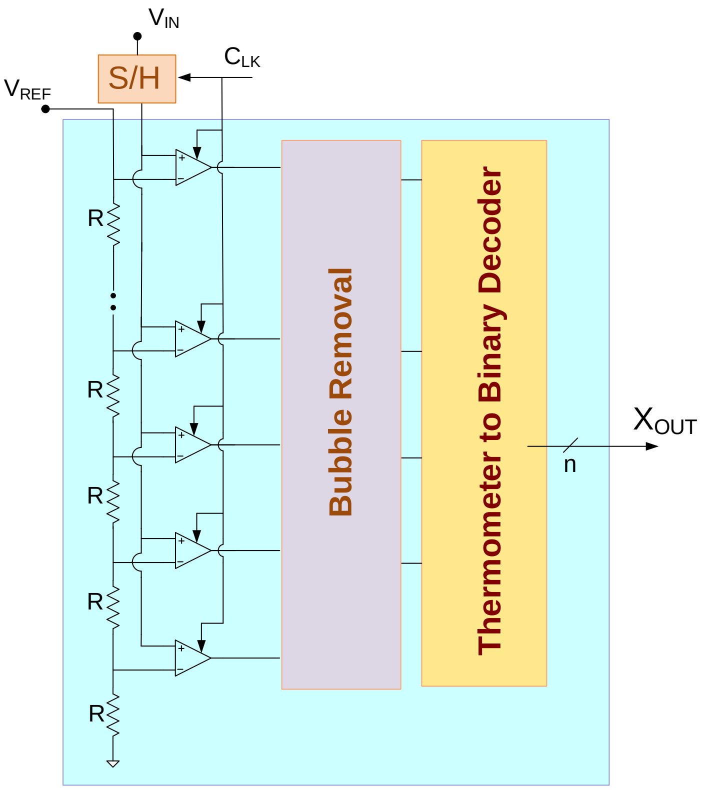


VREF
VIN
R
R
R
R
R
Thermometer to Binary Decoder
XOUT
n



VREF
VIN
R/2
R
R
R
R
R/2
Thermometer to Binary Decoder
XOUT
n

Flash ADC



Basic structure has thermometer code at output

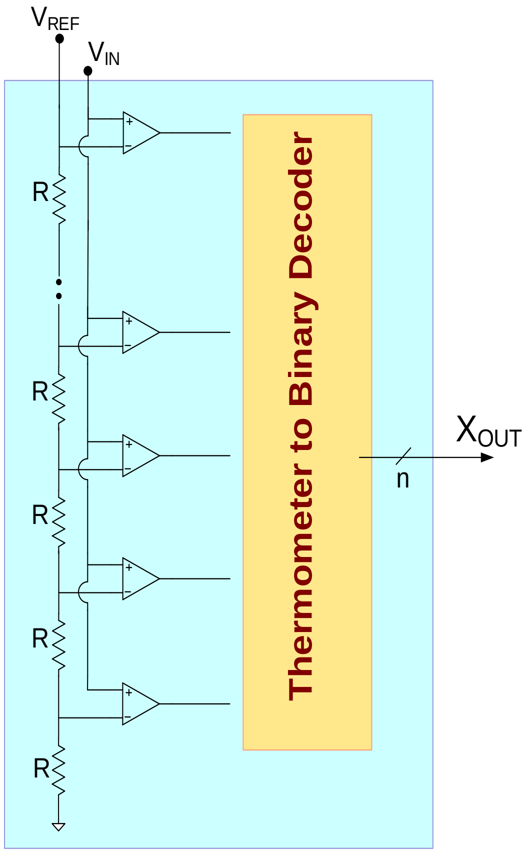
Performance Issues:

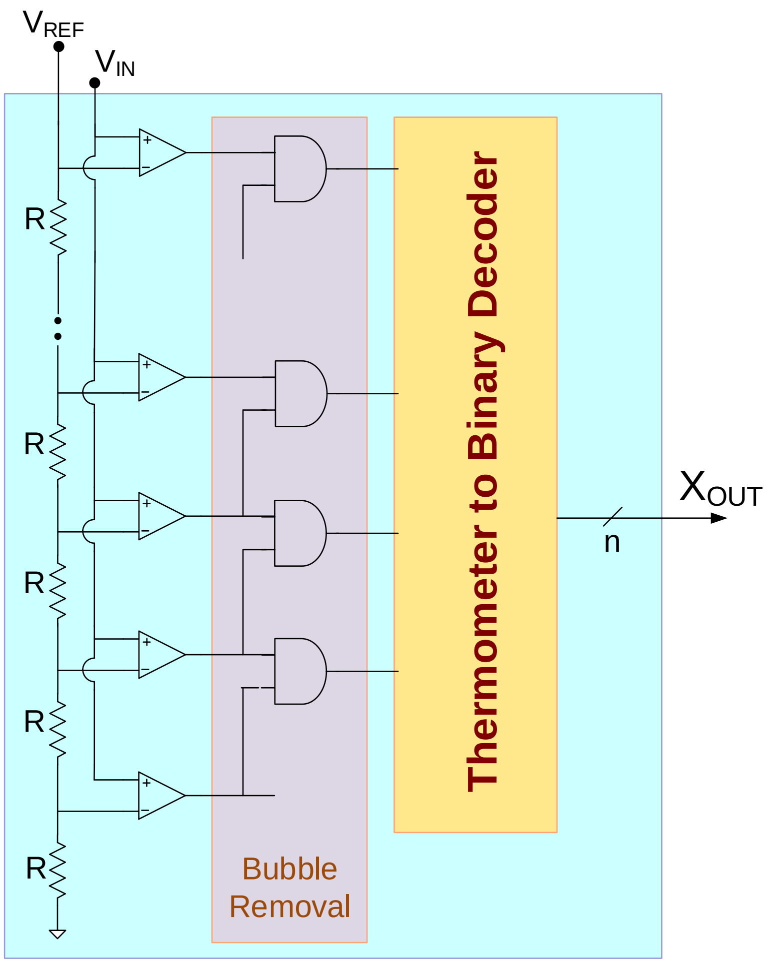
- \+ Very fast
- \+ Simple architecture
- \+ Instantaneous output

 Bubble vulnerability

- − Input change during conversion
- − Offset of comparators
- − Number of components and area (for large n)
- − Speed of comparators
- − Loading of V_{REF} and V_{IN}
- − Propagation of V_{IN} and Kickback
- − Power dissipation (for large n)
- − Layout of resistors
- − Voltage and temperature dependence of R's
- − Matching of R's

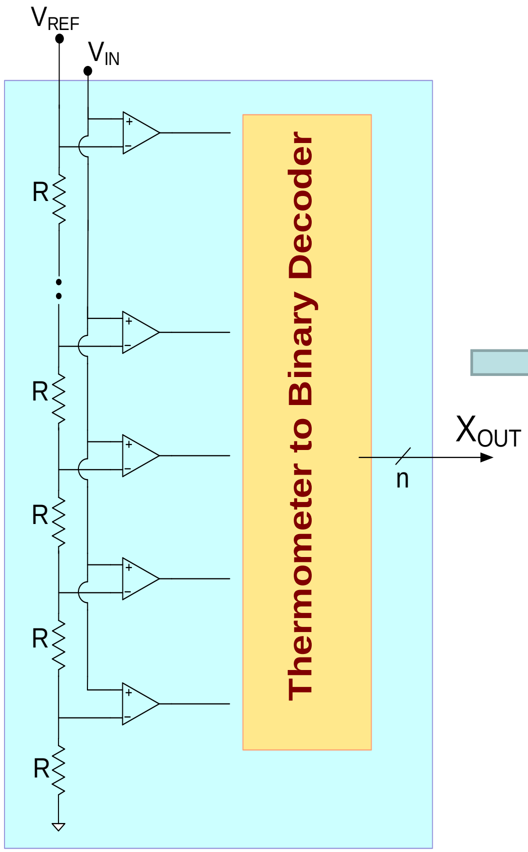
Flash ADC

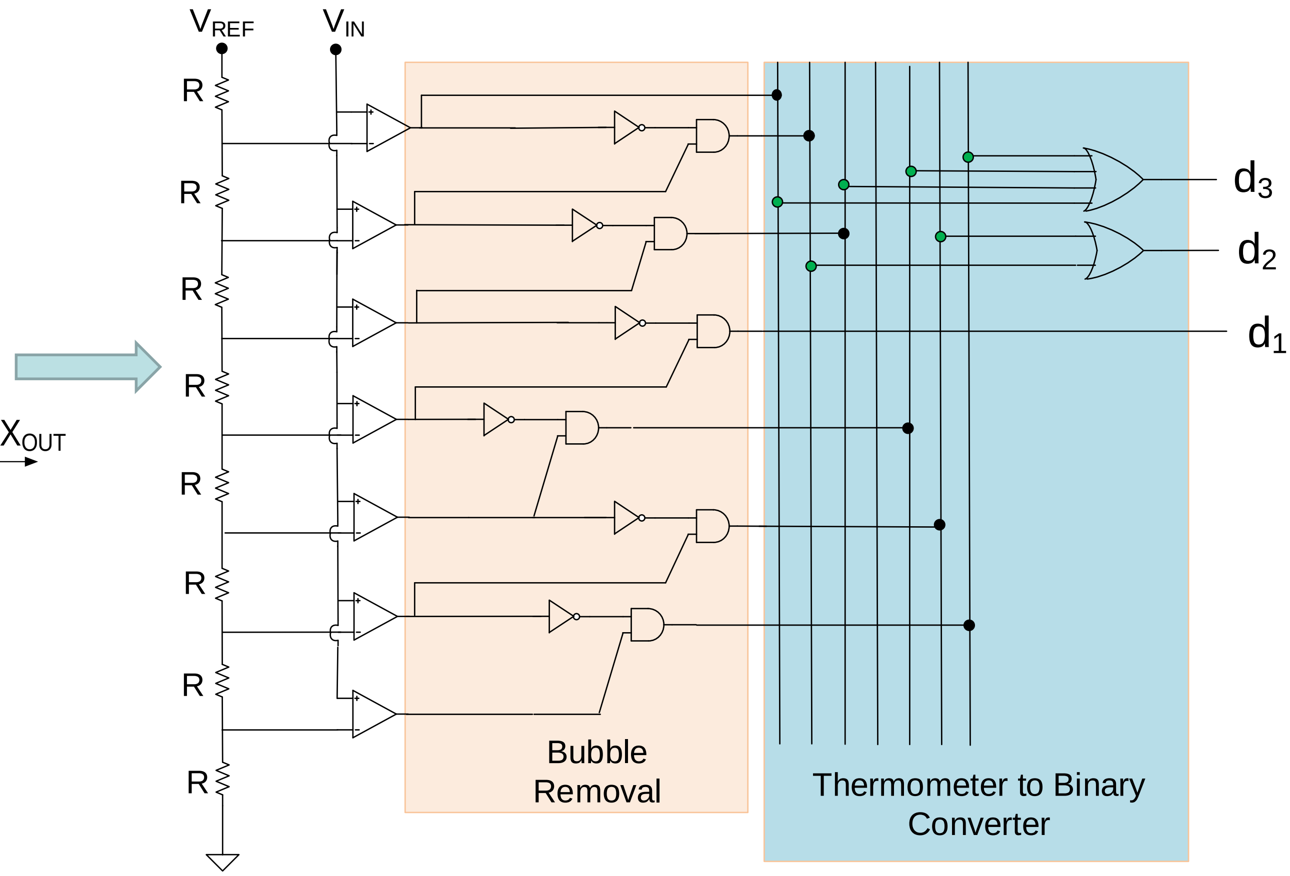




Bubble Removal Approach

Flash ADC





Another Bubble Removal Approach

Stay Safe and Stay Healthy !

End of Lecture 18